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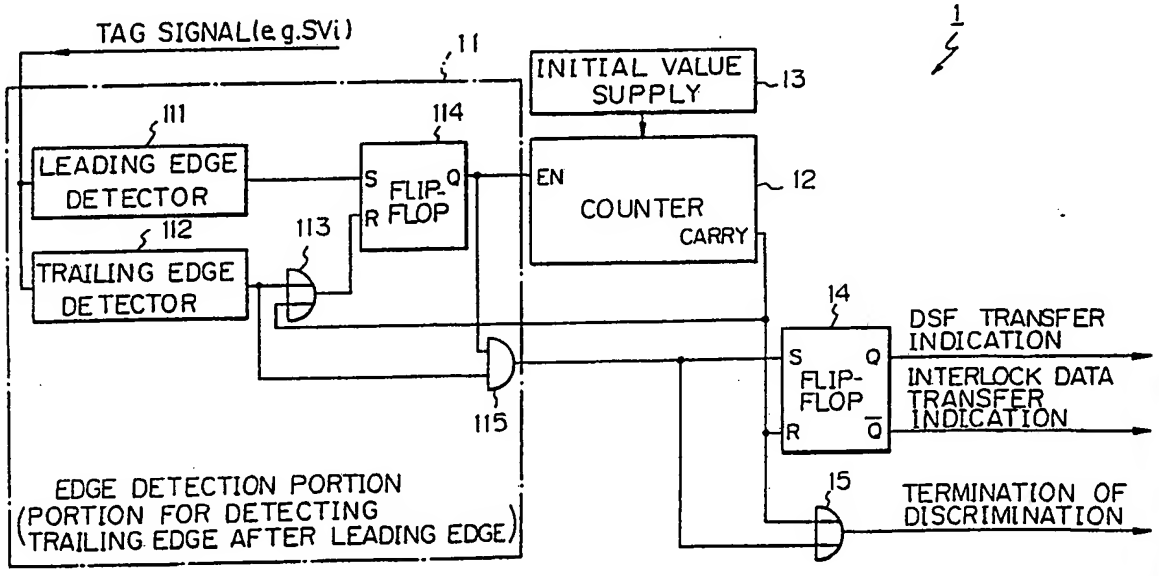
(54) Title: DATA TRANSFER SYSTEM HAVING TRANSFER DISCRIMINATION CIRCUIT



(57) Abstract

In a data transfer system having a transfer discrimination circuit (1) for discriminating the type of data transfer between an input/output channel device and I/O devices for a computer, the transfer discrimination circuit includes an edge detection unit (11) operating in response to a tag signal supplied to the edge detection unit for detecting the trailing edge of the tag signal after a leading edge of the tag signal has passed, the edge detection unit having a leading edge detector (111), a trailing edge detector (112), a storage element (114), and logic gate circuits (113, 115), a timing unit (12, 13) operating in response to the output of the edge detection unit for counting a predetermined time, and a discrimination storage unit (14) operating in response to the output of the timing unit for delivering an output indicating an interlock data transfer or an

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DESCRIPTION

TITLE OF THE INVENTION

Data Transfer System Having Transfer Discrimination Circuit

TECHNICAL FIELD

The present invention is related to a data transfer system having a transfer discrimination circuit. The system according to the present invention is applicable to a usual computer system constituted by a central part at a central location and input/output devices (I/O devices) at remote locations.

BACKGROUND ART

In general, there are two kinds of data transfer used for the channel interface of a computer, i.e., the interlock data transfer with which a maximum transfer speed of 1.5 mega bytes per second is attained for a distance of about 5 to 10 m between the input/output channel device and the input/output device (I/O device), and the data streaming feature (DSF) data transfer with which a maximum transfer speed of 3 mega bytes per second is attained for a distance of about 120 m between the input/output channel device and the I/O device. In the procedure for the signals in the channel interface, there are no rules prescribed by the computer manufacturer for the signal or the procedure which indicates which of these two kinds of data transfer is being used.

Where an arrangement is used for extending the distance between the input/output channel device and the I/O device, it is necessary to discriminate by which data transfer, the interlock data transfer or the DSF data transfer, the data transfer is being carried out, to realize a satisfactory data transfer.

In general, the interface procedure of the input/output channel device is the same for either of these data transfers, and the data transfer is satisfactorily carried out by the input/output channel

device without concern for by which data transfer, the interlock data transfer or the DSF data transfer, the data transfer is being carried out.

However, where the channel interface distance is increased by an insertion of a serially connected transmission line, a distance extension device must be provided in the channel interface without disturbing the usual operation of the channel interface.

Therefore, to coincide the operation of the distance extension device with the I/O device, a problem arises in that it is necessary to discriminate by which data transfer, the interlock data transfer or the DSF data transfer, the data transfer is being carried out.

DISCLOSURE OF THE INVENTION

It is an object of the present invention to provide an improved data transfer system having a transfer type discrimination circuit which is able to discriminate between the interlock data transfer and the DSF data transfer without adverse affect on the operation of the channel interface.

In accordance with an aspect of the present invention, there is provided a data transfer system having a transfer discrimination circuit for discriminating the type of data transfer used between an input/output channel device and I/O devices for a computer, in which the transfer type discrimination circuit includes: an edge detection unit operating in response to a tag signal supplied thereto to detect a trailing edge of the tag signal after a leading edge of the tag signal has passed, the edge detection unit having a leading edge detector, a trailing edge detector, a storage element, and logic gate circuits; a timing unit operating in response to the output of the edge detection unit to count a predetermined length of time; and a discrimination storage unit operating in response to the output of the timing unit to deliver an output indicating one type of data transfer or an output

indicating the other type of data transfer.

BREIF DESCRIPTION OF THE DRAWINGS

In the drawings,

Fig. 1A shows a data transfer system for a computer to which the system according to the present invention is applied;

Fig. 1B shows an exchange of tag signals through signal lines and of data through data buses between the computer side and the I/O device side in the data transfer system of Fig. 1A;

Fig. 2 shows a process of a signal exchange between the I/O device side and the input/output channel device side by the interlock data transfer;

Fig. 3 shows a process of a signal exchange between the I/O device side and the input/output channel device side by the DSF data transfer;

Fig. 4 shows a data transfer system for a computer according to an embodiment of the present invention to which a transfer discrimination circuit is applied;

Fig. 5 shows the structure of a typical transfer discrimination circuit in a data transfer system for a computer according to the embodiment of the present invention shown in Fig. 4;

Figs. 6 and 7 show the waveforms of signals in the transfer discrimination circuit shown in Fig. 5;

Fig. 8 shows a diagram expressing the operation of the transfer discrimination circuit in a data transfer system for a computer according to an embodiment of the present invention, from one viewpoint;

Fig. 9 shows a data transfer system for a computer according to another embodiment of the present invention in which first and second distance extension devices to which a transfer discrimination circuit is applied are provided;

Fig. 10 shows the structure of the first distance extension device used in the data transfer system of Fig. 9;

Fig. 11 shows the structure of the second distance extension device used in the data transfer system of Fig. 9;

Fig. 12 shows a data transfer system for a computer according to a further embodiment of the present invention;

Fig. 13 shows an example of the structure of the leading edge detector;

Fig. 14 shows an example of the structure of the trailing edge detector;

Figs. 15 and 16 show examples of the structure of the tag transmitting circuit;

Fig. 17 shows an example of the structures of the information receiving circuit, the synthesis circuit, and the frame transmitting circuit;

Fig. 18 shows an example of the pattern of a signal frame for transmission; and

Fig. 19 shows an example of the structures of the frame receiving circuit and the separation circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

Before describing the preferred embodiment of the present invention, a prior art data transfer system will be described with reference to Figs. 1A, 1B, 2, and 3. The operation of the system of Fig. 1A is illustrated by the waveforms for the interlock data of Fig. 2 and by the waveforms for the DSF data transfer of Fig. 3.

In the system of Fig. 1A, a data transfer is carried out between the input/output channel device 6 connected to the computer 5, and the input/output terminal devices (I/O devices). As shown in Fig. 1B, the service out signal (SV OUT), the data out signal (DT OUT), and the bus out signal (BUS OUT) are transferred from the computer side to the input/output terminal device side, and the service in signal (SV IN), the data in signal (DT IN), and the bus in signal (BUS IN) are transferred from the input/output terminal device side to the computer side.

The write operation according to the interlock data transfer is illustrated in Fig. 2. The tag signal SV_i, which is delivered from the I/O device and transmitted through the transfer line, is detected by the input/output channel device. Upon receipt of this SV_i, the input/output channel device delivers the signal SV_0 together with 1 byte of data through the bus line. When the I/O device detects this SV_0 from the input/output channel device and receives data sent from the input/output channel device, the I/O device terminates the signal SV_i. When this termination of the signal SV_i is detected by the input/output terminal device, the input/output terminal device terminates the signal SV_0. Thus, a transfer of 1 byte of data is completed. This transfer of 1 byte of data is then repeated.

The operation of the data transfer from the I/O device to the input/output channel device is carried out in the same way. That is, when the signal SV_i is transmitted from the I/O device to the input/output channel device, a transmission of 1 byte of data is carried out.

In Fig. 3, the operation according to the DSF data transfer is illustrated. The tag signal SV_i is delivered from the I/O device to request a supply of data. The I/O device maintains the SV_i in an ON state for a predetermined time and terminates the SV_i, without awaiting the delivery of SV_0 from the input/output channel device. This predetermined time of the ON state of the SV_i is more than about 270 ns. After an elapse of an OFF state of the SV_i of a predetermined time, for example, a minimum 270 ns, a signal SV_i is again delivered. After an elapse of an ON state of the SV_i of the same predetermined time as described before, the SV_i is terminated. This sequence of operations is then repeated.

The operation of the input/output channel device is the same as the operation in the case of the interlock

data transfer system. Upon receipt of SV_i from the I/O device, the input/output channel device delivers a signal SV_0 and data toward the I/O device. After an elapse of about 270 ns, the termination of SV_i is detected. Upon detection of this termination of SV_i, the signal SV_0 is terminated. This sequence of operations is then repeated.

The input/output device does not terminate the delivery of SV_i in accordance with the detection of SV_0 but independently of the detection of SV_0. In the data streaming type system, when only the signal SV_i is used, the data transfer is not carried out during the period A of the signal SV_i. Accordingly, to increase the efficiency of the transfer of data, the signal DT_i is used in addition to the signal SV_i.

A data transfer system for a computer according to an embodiment of the present invention to which a transfer discrimination circuit is applied is shown in Fig. 4. The structure of a typical transfer discrimination circuit in this data transfer system is shown in Fig. 5.

The system of Fig. 4 is constituted by a computer 5, an input/output channel device 6, input/output terminal devices (I/O devices) 71, 72, 73 ..., an additional device 81 for distance extension at the input/output channel device side, and an additional device 82 for distance extension at the I/O device side. A transfer discrimination circuit 1 is provided in the additional device 82.

The transfer discrimination circuit 1 shown in Fig. 5 includes an edge detection portion 11 having a leading edge detector 111, a trailing edge detector 112, an OR gate 113, a flip-flop circuit 114, and an AND gate; a counter 12, an initial value supply portion 13, a flip-flop circuit 14, and an OR gate 15.

The leading edge detector 111 receives a tag signal such as SV_i and delivers an output signal to the set

input terminal of the flip-flop circuit 114. The trailing edge detector 112 receives a tag signal such as SV_i and delivers an output signal to an OR gate 113 and the AND gate 115. The output of the OR gate 113 is supplied to the reset input terminal of the flip-flop circuit 114, and the output of the flip-flop circuit 114 is supplied to the AND gate 115.

Through the enable input terminal, the counter 12 receives the output of the flip-flop circuit 114, and delivers the output signal to the reset input terminal of the flip-flop circuit 14 and the OR gate 15. The output of the AND gate 115 is supplied to the set input terminal of the flip-flop circuit 14 and the AND gate 15. The Q output terminal of the flip-flop circuit 14 delivers a signal indicating a DSF data transfer. The $\bar{Q}$ (barred Q) output terminal of the flip-flop circuit 14 delivers a signal indicating a interlock data transfer. The OR gate 15 delivers a signal indicating the termination of the discrimination.

The operation of the transfer discrimination circuit 1 of Fig. 5 in the case of the interlock data transfer will be described with reference to Fig. 6. A tag signal SV_i is supplied to the leading edge detector 111 and the trailing edge detector 112 (Fig. 6, (1)). The output signal of the leading edge detector 111 is supplied to the flip-flop circuit 114 (Fig. 6, (2)). The potential of the output of the trailing edge detector 112 is maintained at the LOW level. (Fig. 6, (3)). The enable input signal is still supplied to the counter 12 (Fig. 6, (4)). The potential of the output signal of the AND gate 115 is maintained to be LOW (Fig. 6, (5)). After a relatively long time such as 2 μs, a carry signal indicating an overflow of the counter is delivered from the counter 12 (Fig. 6, (6)). The flip-flop circuits 114 and 14 are reset by this carry signal to initialize the counter 12. When the flip-flop circuit 14 is reset, the signal of a HIGH

potential is delivered from $\bar{Q}$ output terminal of the flip-flop circuit 14 (Fig. 6, (7)). This signal of a HIGH potential from $\bar{Q}$ output terminal indicates an interlock data system.

The operation of the transfer discrimination circuit 1 of Fig. 5 in the case of the DSF data transfer will be described with reference to Fig. 7. A tag signal SV_i is supplied to the leading edge detector 111 and the trailing edge detector 112 (Fig. 7, (1)). The output of the leading edge detector 111 is supplied to the set input terminal of the flip-flop circuit 114 (Fig. 7, (2)). The output of the trailing edge detector 112 is supplied to the reset input terminal of the flip-flop circuit 114 and the AND gate 115 (Fig. 7, (3)). The enable signal is still supplied to the counter 12 from the leading edge detect pulse to the trailing edge detect pulse (Fig. 7, (4)). The counter 12 carries out a counting from the initial value previously supplied from the initial value supply portion 13. When the trailing edge detector 112 delivers the trailing edge detect pulse (Fig. 7, (3)), a HIGH potential signal from the AND gate 115 is supplied to the set input terminal of the flip-flop circuit 14 (Fig. 7, (5)) to cause a delivery of a HIGH potential output signal from Q output terminal of the flip-flop circuit 14 (Fig. 7, (6)). This HIGH potential signal from the Q output terminal indicates the DSF data transfer.

The flip-flop circuit 114 is reset by the output signal of the trailing edge detector 112 supplied to the reset input terminal of the flip-flop circuit 114 so that the counter 12 terminates the counting and returns to the initial state.

The initial value of the counter 12 is selected by the initial value supply portion 13. The initial value of the counter is a value such that an overflow of the count value occurs upon completion of a counting operation for a time corresponding to a predetermined time.

From one point of view, the data transfer discrimination circuit used in the present invention may also be expressed by a diagram shown in Fig. 8. The data transfer discrimination circuit shown in Fig. 8 is constituted by a DSF data transfer detection portion, an interlock data transfer detection portion, and a storage portion. The DSF data transfer portion receives a tag signal and the output of the interlock data transfer detection portion. The interlock data transfer detection portion receives the output of the DSF data transfer detection portion. The storage portion receives the outputs of the DSF data transfer detection portion and the interlock data transfer detection portion, and delivers either an output for a DSF data transfer or an output for an interlock data transfer.

According to the viewpoint shown in Fig. 8, a data transfer discrimination circuit used for a data transfer between an input/output channel device and I/O devices for a computer is constituted by a DSF data transfer detection portion for detecting a DSF data transfer by delivering an output as the result of detecting that the time between the leading edge and the trailing edge of a first tag signal transmitted from an I/O device to the input/output channel device falls within a predetermined time; an interlock data transfer detection portion for detecting an interlock data transfer by delivering an output as the result of detecting that the trailing edge of a first tag signal transmitted from an I/O device to the input/output channel device is not detected within the predetermined time after the leading edge of the first tag signal; and a storage portion for storing the output of the DSF data transfer detection portion or the output of the interlock data transfer detection portion.

A data transfer system for a computer according to another embodiment of the present invention is shown in Fig. 9. The structure of the No. 1 distance extension device used in the system of Fig. 9 is shown in Fig. 10,

and the structure of the No. 2 distance extension device used in the system of Fig. 9 is shown in Fig. 11.

The system of Fig. 9 is constituted by a computer 5, an input/output channel device 6, a No. 1 distance extension device 2, a transmission line 3, a No. 2 distance extension device 4, and I/O devices 71, 72, 73 ... Parallel signals from the input/output channel device 6 are converted to a serial signal having a predetermined format by the No. 1 distance extension device 2, and the converted serial signal is transmitted through the transmission line 3 to the No. 2 distance extension device 4 in which the transmitted signal is again converted to the original parallel signals which are supplied to the I/O devices 71, 72, 73, ... The data transmission from the I/O devices 71, 72, 73 ... to the computer 5 is carried out in the same way.

In the system shown in Fig. 9, inter-channel distance extension devices are used for connecting I/O devices at locations remote from the host computer. To extend the inter-channel distances, the No. 1 distance extension device is and the No. 2 distance extension device are arranged.

As shown in Fig. 10, the No. 1 distance extension device 2 is constituted by a channel interface input/output portion 21, a transfer receiving and switching portion 23, a sequence conversion portion 22, and a CPU 24. The channel interface input/output portion 21 includes a tag receiving circuit 211, a tag transmitting circuit 212, and a transfer data input/output control portion 213. The transfer receiving and switching portion 23 includes an information receiving circuit 232, and a separation circuit. The sequence conversion portion 22 includes a frame receiving circuit 221, a frame transmitting circuit 222, a data block transfer control circuit 223, and a data buffer 224.

As shown in Fig. 11, the No. 2 distance extension

device 4 is constituted by a sequence conversion portion 42, a transfer determination portion 43, a channel interface input/output portion 41, and a CPU 44. The sequence conversion portion 42 includes a frame transmitting circuit 421, a frame receiving circuit 422, a data block transfer control circuit 423, and a data buffer 424. The transfer determination portion 43 includes a transfer discrimination portion 1, a synthesis circuit 431, an information receiving circuit 432, and a tag transmitting circuit 433. The channel interface input/output portion 41 includes a tag receiving circuit 411 and a transfer data input/output control circuit 412.

The operation of the devices of Figs. 10 and 11 will be described. In the No. 2 distance extension device 4, a data transfer is carried out after a selection of an I/O device. The tag receiving circuit 411 is informed of the commencement of a data transfer by the CPU 44, which is monitoring the state of signals during the process. The tag receiving circuit 411 then drives the switch 433a to switch off the connection between the tag receiving circuit 411 and the tag transmitting circuit 433.

The leading edge of the signal TAG_i , which is first supplied from an I/O device to the tag receiving circuit 411 during the data transfer, is detected by the transfer discrimination portion 1. However, since the switch 433a is OFF, the signal TAG_0 corresponding to the signal TAG_i is not transmitted from the tag transmitting circuit 433.

In this situation, if the data transfer of the I/O device is carried out in the interlock data transfer, the signal TAG_0 is not transmitted, the signal TAG_i remains in at a HIGH potential, and the trailing edge of the signal TAG_0 can not be detected. However, in the DSF data transfer, when a predetermined time has passed, the I/O device independently carries out a switching-off

operation, and accordingly, the trailing edge of the signal can be detected.

While the detection operation is proceeding, the switch 433a is in an OFF state. When the deteaction operation is completed, the switch 433a is made ON to enable communication between the I/O device and the No. 2 distance extension device 4.

When the transfer discrimination portion 1 detects that the present transfer is a DSF data transfer, a signal is generated in a predetermined form in the information receiving circuit 432 which generates information about the transfer, and a signal synthesis with the parallel data from the data buffer 424 is carried out in the synthesis circuit 431. The output of the synthesis circuit 431 is supplied to the frame transmitting circuit 421 in which the signals are converted to a series signal which is transmitted to the No. 1 distance extension device 2.

In the No. 1 distance extension device 2, the received signal is converted to parallel signals in the frame receiving circuit 221, and the DSF data transfer detection information is separated from the output of the frame receiving circuit 221 in the separation circuit 231. The separated DSF data transfer detection information is detected by the information receiving circuit 232, and the tag receiving circuit 411 and the tag transmitting circuit 433 are switched to become a tag receiving and transmitting circuit for a DSF data transfer by a switch (not shown). Note, when the information indicates an interlock data transfer, this switching is not carried out.

A data transfer system for a computer according to a further embodiment of the present invention is shown in Fig. 12. The system of Fig. 12 includes a No. 1 tag response circuit 81 which is operated with a normal timing for the tag signal TAG_i from the I/O device, a No. 2 tag response circuit 82, which is operated at a

timing delayed from the normal timing for the tag signal TAG_i from the I/O device, a selection circuit 83, a counter circuit 85 for control, and a data transfer discrimination portion 1. The data transfer discrimination portion 1 in the system of Fig. 12 is fundamentally the same as the device of Fig. 5.

One of the No. 1 tag response circuit 81 and No. 2 tag response circuit 82 is selected by the selection circuit 83, so that one of the outputs from the No. 1 tag response circuit 81 and No. 2 tag response circuit 82 is supplied as the tag signal TAG_0 from the selection circuit 83 to the I/O device side 7.

The counter circuit 85 for control periodically operates the selection circuit 83 and the transfer discrimination portion 1. The counter circuit 85 is, for example, a time measuring counter which counts, for example, a time of 1 ms. In the counter circuit 85, for example, one count is carried out per one hundred tag signals SV_i.

The operation of the system of Fig. 12 will be described. It is presumed that the selection of I/O devices and the data transfer concerning command transmission has been completed as the preliminary processing.

First, the selection terminal device makes the potential of SV_i or DT_i as the tag signal HIGH, and, in accordance with this tag signal TAG_i, only one of the No. 1 tag response circuit 81 and the No. 2 tag response circuit 82 is operated.

That is, when the counter circuit 85 for control is delivering a LOW level potential signal as an OFF signal, the selection circuit 83 operates the No. 1 tag response circuit 81, and the tag signal TAG_i is supplied as a response tag signal TAG_0 to the I/O device without delay. Conversely, when the counter circuit 85 for control is delivering a HIGH level potential signal as an ON signal, the selection circuit 83 operates the

No. 2 tag response circuit 82 and the transfer discrimination portion 1.

Thus, the OFF signal from the counter circuit 85 for control operates as a selection instruction signal from the No. 1 tag response circuit 81 to the selection circuit 83, and the ON signal from the counter circuit 85 for control operates as a selection instruction signal from the No. 2 tag response circuit 82 to the selection circuit 83 as well as an operation instruction signal to the transfer discrimination circuit 1.

The transfer discrimination portion 1 receives the operation instruction signal from the counter circuit 85 for control and, based on the tag signal TAG_i from the I/O device, carries out a discrimination between the DSF data transfer and the interlock data transfer. During that discrimination operation, the response to the tag signal TAG_i in the No. 2 tag response circuit is delayed.

Upon completion of the discrimination between the DSF data transfer and the interlock data transfer, the transfer discrimination portion 1 delivers either a DSF data transfer indication signal or an interlock data transfer indication signal, as a result of the discrimination, and supplies the No. 2 tag response circuit 82 with the discrimination termination signal. As a result, the No. 2 tag response circuit 82 supplies the response signal TAG_0 of the tag signal TAG_i to the I/O device. In other words, the tag response is delayed.

Upon completion of the operation, the transfer discrimination circuit 1 supplies the No. 2 tag response circuit 82 with the discrimination termination signal, and as a result, the No. 2 tag response circuit 82 supplies the response signal TAG_0 to the I/O device through the selection circuit 83 in response to the tag signal TAG_i from the I/O device.

Thus, the data transfer from the I/O device side to No. 2 distance extension device is periodically discriminated.

An example of the structure of the leading edge detector 111 in the system of Fig. 5 is shown in Fig. 13. An example of the structure of the trailing edge detector 112 in the system of Fig. 5 is shown in Fig. 14; an example of the structure of the tag transmitting circuit 212 in the system of Fig. 10 is shown in Fig. 15; and an example of the structure of the tag transmitting circuit in the system of Fig. 11 is shown in Fig. 16. Examples of the structures of the information receiving circuit, the synthesis circuit, and the frame transmitting circuit in the system of Fig. 11 are shown in Fig. 17. An example of pattern of a signal frame for transmission for the circuit of Fig. 17 is shown in Fig. 18, and examples of the structures of the frame receiving circuit and the separation circuit are shown in Fig. 19.

The leading edge detector shown in Fig. 13 is constituted by first and second flip-flop circuits and an AND gate. The first flip-flop circuit receives an input signal, for example, SV_i , and a clock signal. The second flip-flop circuit receives a Q output of the first flip-flop circuit and the clock signal. The AND gate receives a Q output signal of the first flip-flop circuit and a $\bar{Q}$ output signal of the second flip-flop circuit. The AND gate delivers the leading edge indication signal.

The trailing edge detector shown in Fig. 14 is constituted by first and second flip-flop circuits and an AND gate. The first flip-flop circuit receives an input signal, for example, SV_i , and a clock signal. The second flip-flop circuit receives a Q output of the first flip-flop circuit and the clock signal. The AND gate receives a $\bar{Q}$ output signal of the first flip-flop circuit and a Q output signal of the second flip-flop circuit. The AND gate delivers the trailing edge indication signal.

The tag transmitted circuit shown in Fig. 15 is

constituted by gate Nos. 1 to 8, a flip-flop circuit, a pulse width ensuring circuit, and a driver. In the operation of the circuit of Fig. 15, first the interlock data transfer indication signal is supplied from the information receiving circuit. The gate Nos. 1 and 2 check this condition. When the result of the check is affirmative, the TAG_i set circuit constituted by gate Nos. 3 to 5 and the TAG_i reset circuit constituted by gate Nos. 6 to 8 are enabled. In the case of an interlock data transfer, the set condition is established by gate Nos. 3 and 5, and the reset condition is established by gate Nos. 6 and 8. In the case of a DSF data transfer, the set condition is established by gate Nos. 4 and 5, and the reset condition is established by gates 7 and 8. In the case of a DSF data transfer, the pulse width ensuring circuit ensures the ON/OFF time of a pulse, and upon termination of the need to ensure the ON/OFF time, the output of the device is made ON.

The tag transmitting circuit shown in Fig. 16 is constituted by a flip-flop circuit for TAG_0 output requests, a flip-flop circuit for TAG_0 holds, gate Nos. 1 to 4, a pulse width ensuring circuit, and a driver. In the operation of the circuit of Fig. 16, the flip-flop circuit for TAG_0 output requests is set by the received TAG_i. When the DSF detection operation is completed, the output request signal is delivered from gate No. 1. When the stop conditions are absent and the bus c :put signal allowed is received for establishing a timing, gate No. 4 is made ON, and subsequently, gate No. 2 is made ON. Therefore, the flip-flop circuit for TAG_0 holds is set, and accordingly, the output signal is delivered from the device. With regard to the flip-flop circuit for TAG_0 holds, the pulse width is ensured by the pulse width ensuring circuit. When the input TAG_i is made OFF, the flip-flop circuit for TAG_0 holds is reset by the function of gate No. 3.

As shown in Fig. 17, the frame transmitting circuit

includes a frame data request circuit, a parallel serial conversion circuit, a frame synchronization and frame formation circuit, and a driver, the synthesis circuit includes a register, and the information receiving circuit includes a flip-flop circuit.

The signal frame for transmission having the pattern shown in Fig. 18 is serially transmitted between the first and second distance extension devices. A specific bit in the control portion in the frame is defined as the DSF transfer information.

In the operation of the circuits shown in Fig. 17, detection of a DSF data transfer is transmitted to the flip-flop circuit in the information receiving circuit and is stored therein as information. The frame transmitting circuit is then operated by the CPU, commences to construct the frame structure of the signal, and continues to carry out the transmission operation until receiving a termination instruction from the CPU. The data from the data buffer is loaded to the register for constructing the frame in the synthesis circuit based on the signal from the frame data request circuit, and the output of the flip-flop circuit for holding DSF transfer information is set in the bit position of the DSF transfer information in the frame. In the frame transmitting circuit, the frame data formed as described above is loaded in the parallel/serial circuit, and the output of the parallel/serial circuit is delivered to the transmission line, while maintaining the frame synchronization of the frame data. The above-described processes are then repeated.

As shown in Fig. 19, the frame receiving circuit includes a receiver, a clock synchronization circuit, a frame synchronization circuit, and a serial/parallel circuit, and the separation circuit includes a register.

CLAIMS

1. A data transfer system having a transfer discrimination circuit for discriminating data transfer between an input/output channel device and input/output devices for a computer, said transfer discrimination circuit comprising:

edge detection means operating in response to a tag signal supplied to said edge detection means for detecting a trailing edge of the tag signal after a leading edge of the tag signal has passed, said edge detection means having a leading edge detector, a trailing edge detector, a storage element, and logic gate circuits;

timing means operating in response to an output of said edge detection means for counting a predetermined time; and

discrimination storage means operating in response to the output of said timing means for delivering an output indicating one type of data transfer or an output indicating another type of data transfer.

2. A system according to claim 1, wherein said storage element in said edge detection means is a flip-flop circuit.

3. A system according to claim 2, wherein the set input terminal of said flip-flop circuit receives the output of said leading edge detector, and the reset input terminal of said flip-flop circuit receives the output of said trailing edge detector through an OR gate.

4. A system according to claim 2, wherein the output of said flip-flop circuit is supplied to an enable input terminal of said timing means.

5. A system according to claim 1, wherein said timing means receives an initial value from an initial value supply means.

6. A system according to claim 1, wherein said discrimination storage means is a flip-flop circuit.

7. A system according to claim 6, wherein the set input terminal of said flip-flop circuit receives the output of an AND gate in said edge detection means, said AND gate receiving the output of the storage element and the output of said trailing edge detector in said edge detection means.

8. A system according to claim 6, wherein the reset input terminal of said flip-flop circuit receives the output of said timing means.

9. A data transfer discrimination circuit used for a data transfer between an input/output channel device and input/output devices for a computer, said circuit comprising:

data streaming feature (DSF) data transfer detection means for detecting a data streaming feature data transfer by delivering an output as the result of a detection that the time between the leading edge and the trailing edge of a first tag signal transmitted from an input/output device to the input/output channel device falls within a predetermined time;

interlock data transfer detection means for detecting an interlock data transfer by delivering an output as the result of a detection that the trailing edge of a first tag signal transmitted from an input/output device to the input/output channel device is not detected within said predetermined time after the leading edge of the first tag signal; and

storage means for storing the output of said data streaming feature transfer detection means or the output of said interlock data transfer detection means.

10. A system according to claim 1, further comprising a first distance extension device connected between said input/output channel device and a transmission line extending to the input/output devices, and a second distance extension device connected between said transmission line and the input/output devices,

said transfer discrimination circuit being included in said second distance extension device.

11. A data transfer system using a channel interface distance extension device having a transfer discrimination circuit for discriminating a data transfer between an input/output channel device and input/output devices for a computer, said system comprising first and second distance extension means arranged between the input/output channel device and the input/output devices,

said first and second distance extension means comprising sequence conversion means in which signals transmitted from the input/output channel device or the input/output devices through a first or a second channel interface input/output circuit in accordance with a channel interface sequence are converted into signals with a predetermined format and the converted signals are serially transmitted, or the received signals with the predetermined format are reversely converted and the obtained data is transmitted to the input/output channel device or the input/output devices in accordance with the channel interface sequence,

said second distance extension means comprising transfer determination means for determining whether the data transfer of an input/output device in question is an interlock data transfer or a data streaming feature data transfer by using a tag delivered first from said input/output device during the period of data transfer,

said first distance extension means comprising transfer receiving and switching means for receiving the result of the detection in said transfer determination means and switching the operation of the first channel interface input/output circuit between the interlock data transfer and the data streaming feature data transfer.

12. A system according to claim 1, further

comprising a first tag response circuit for receiving a tag from the input/output devices, a second tag response circuit for receiving the tag from the input/output devices and a discrimination termination signal from the data transfer discrimination circuit, a counter circuit for control of a delivery of a control output, and a selection circuit for receiving the outputs of said first and second tag response circuits and delivering either the output of said first tag response circuit or the output of said second tag response circuit as a tag to the input/output devices in accordance with the control output of said counter circuit as a selection instruction, the delivery of either the output for the data streaming feature data transfer or the output for the interlock data transfer from said data transfer discrimination circuit being controlled by the control output of said counter circuit as an operation instruction.

13. A data transfer system using a channel interface distance extension device arranged between the input/output channel device and the input/output devices for a computer, said channel interface distance extension device comprising:

tag response means for receiving a tag signal from the input/output devices to the input/output channel device and supplying the input/output devices with a response signal responding to the received tag signal,

data transfer discrimination means for receiving a tag signal from the input/output devices to the input/output channel device and discriminating whether the data transfer of a channel interface in question is an interlock data transfer or a data streaming feature data transfer, and

control means for supplying an operation instruction signal at predetermined cycle periods to said data transfer discrimination means.

14. A system according to claim 13, wherein said tag response means comprises a first tag response circuit operating at a normal timing for the tag signal from the input/output device to the input/output channel device,

a second tag response circuit operating with a delay from the normal timing of the operation of said first tag response means, and

a selection circuit for selecting either the output of said first tag response circuit or the output of said second tag response circuit,

the operation of said data transfer discrimination means being terminated when the output of said first tag response circuit is selected in said selection circuit by the control signal from said control means, and the operation of said data transfer discrimination means being executed when the output of said second tag response circuit is selected in said selection circuit by the control signal from said control means.

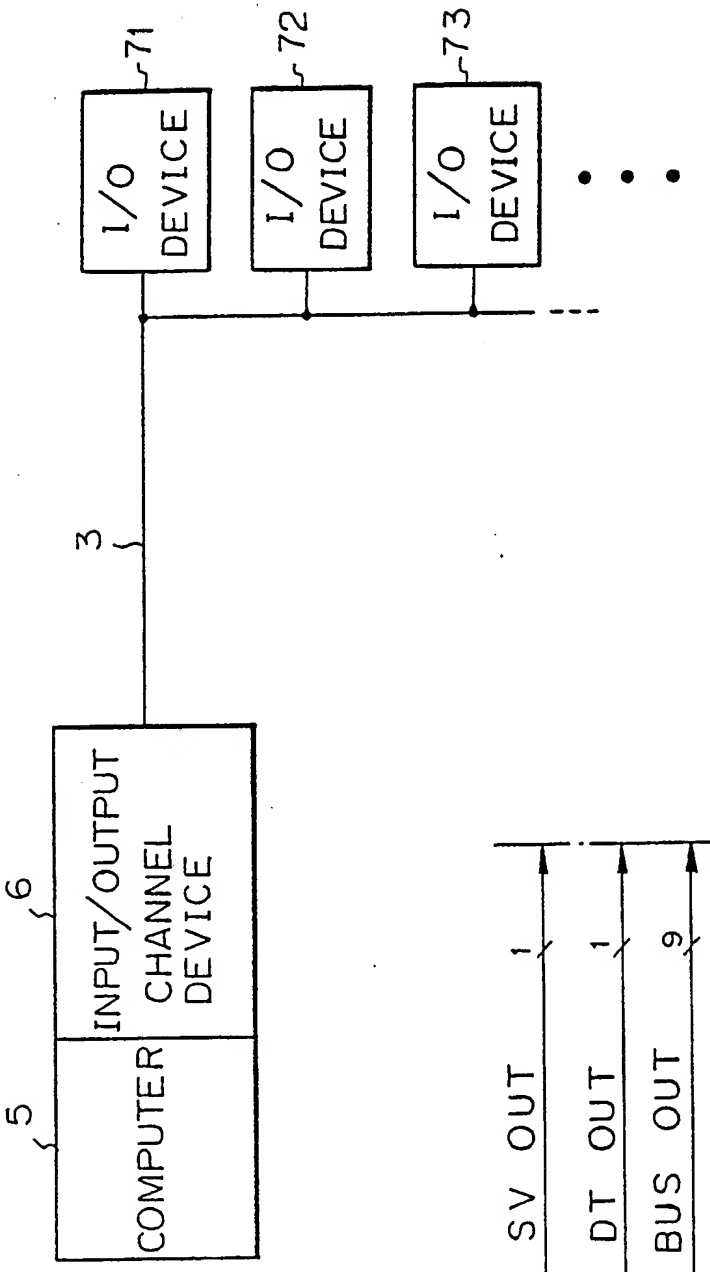

I/O DEVICE
71
I/O DEVICE
72
I/O DEVICE
73
3
INPUT/OUTPUT CHANNEL DEVICE
6
COMPUTER
5

Fig. 1A

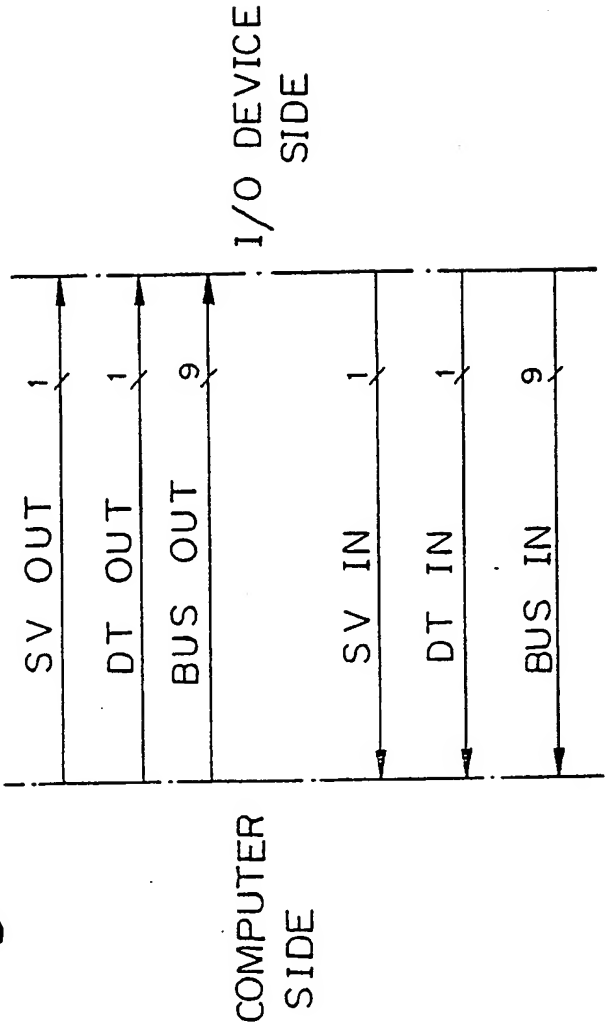

I/O DEVICE SIDE
SV OUT
1
DT OUT
1
BUS OUT
9
SV IN
1
DT IN
1
BUS IN
9
COMPUTER SIDE

Fig. 1B

Fig. 2 INTERLOCK DATA TRANSFER

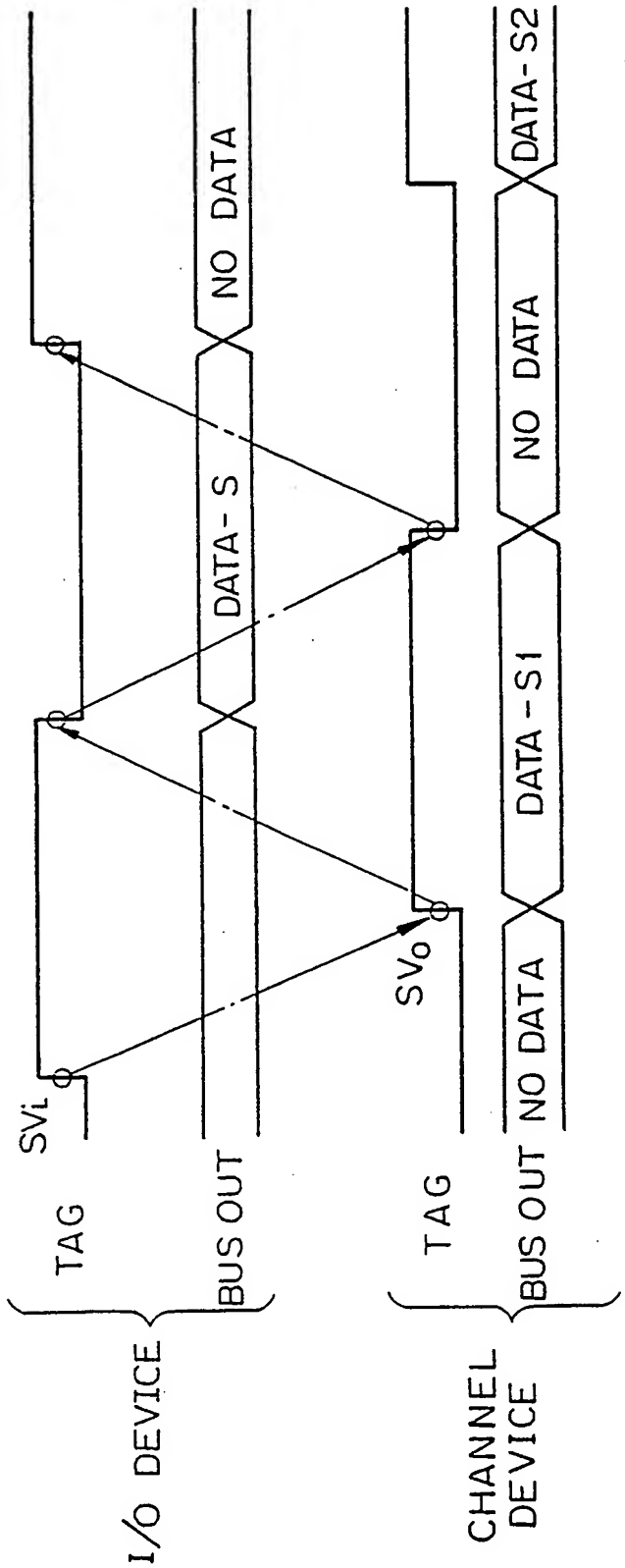


Fig. 3 DATA STREAMING FEATURE (DSF) TRANSFER

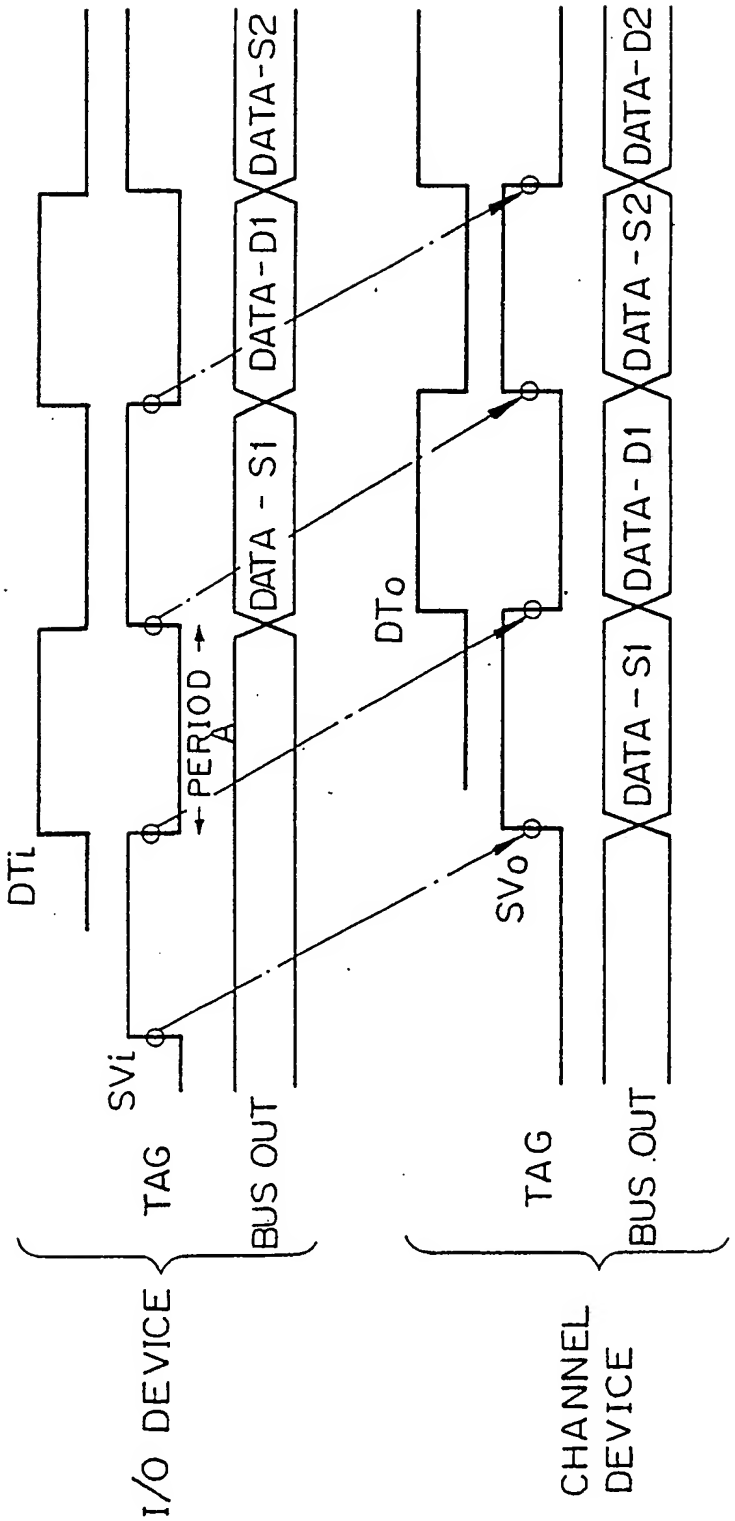


Fig. 4

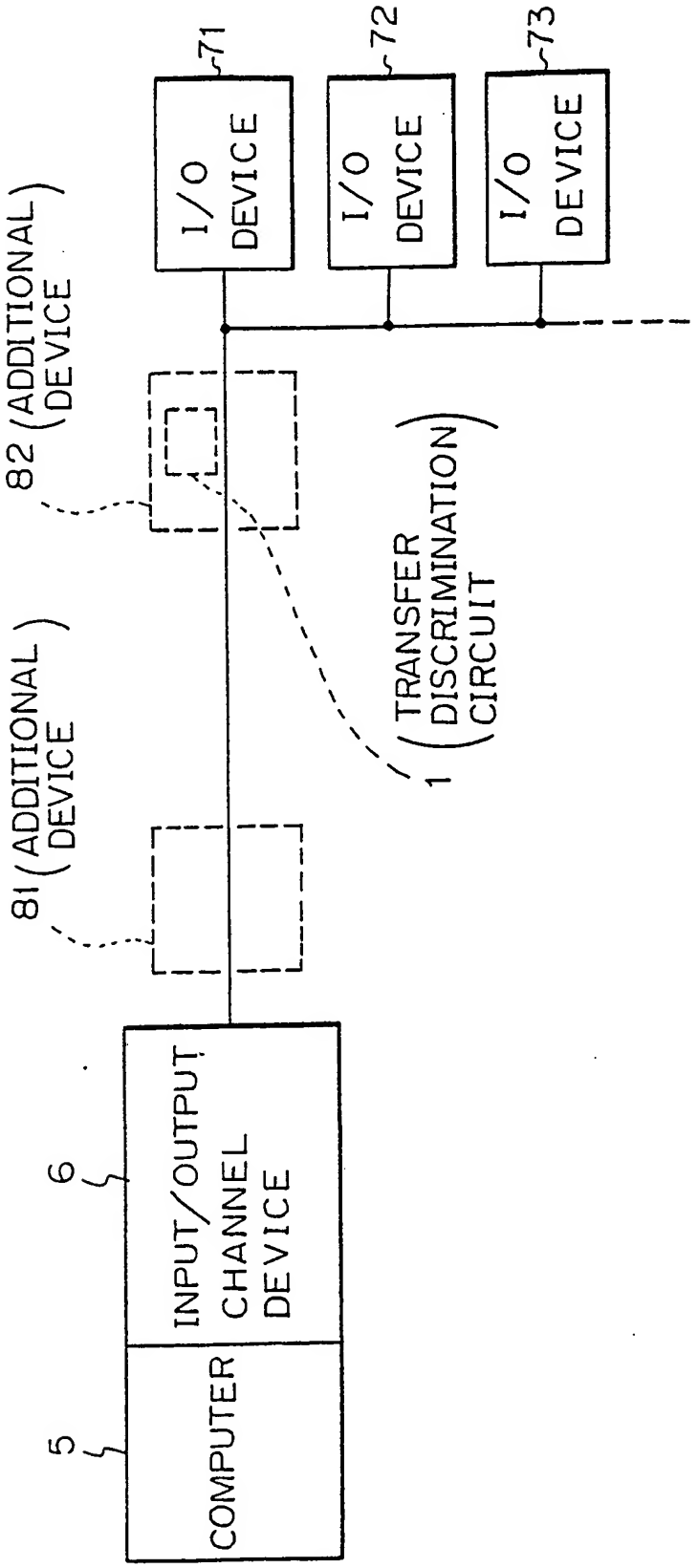

I/O DEVICE
71
I/O DEVICE
72
I/O DEVICE
73
82 (ADDITIONAL DEVICE)
81 (ADDITIONAL DEVICE)
1 (TRANSFER DISCRIMINATION CIRCUIT)
6
INPUT/OUTPUT CHANNEL DEVICE
5
COMPUTER

Fig. 5

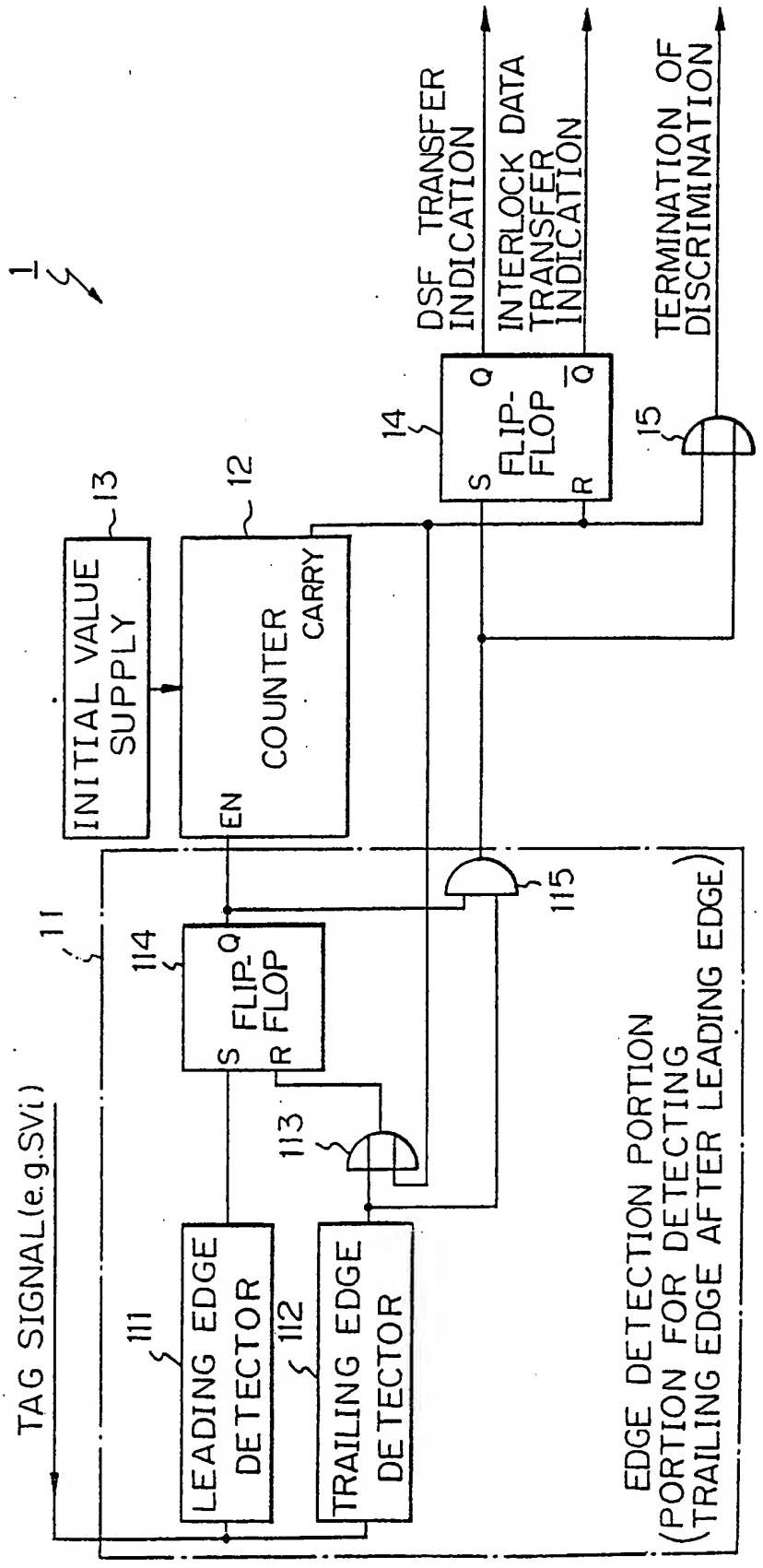

1
TAG SIGNAL(e.g.SVi)
11
EDGE DETECTION PORTION
(PORTION FOR DETECTING
TRAILING EDGE AFTER LEADING EDGE)
111
LEADING EDGE
DETECTOR
112
TRAILING EDGE
DETECTOR
113
114
S
R
FLIP-
FLOP
Q
115
INITIAL VALUE
SUPPLY
13
12
EN
COUNTER
CARRY
14
S
R
FLIP-
FLOP
Q
$\overline{Q}$
15
DSF TRANSFER
INDICATION
INTERLOCK DATA
TRANSFER
INDICATION
TERMINATION OF
DISCRIMINATION

Fig. 6

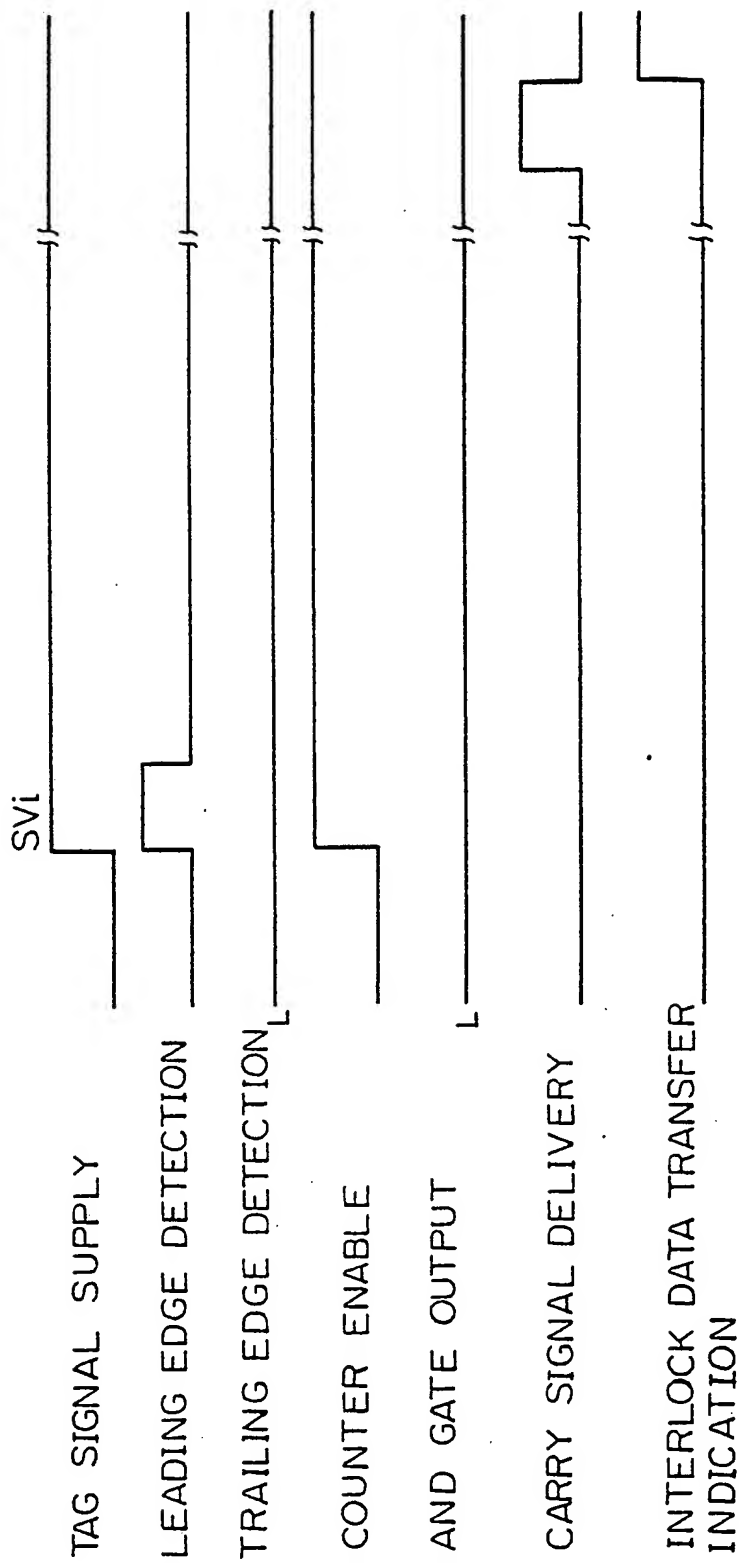

SVi
(1) TAG SIGNAL SUPPLY
(2) LEADING EDGE DETECTION
(3) TRAILING EDGE DETECTION
L
(4) COUNTER ENABLE
(5) AND GATE OUTPUT
L
(6) CARRY SIGNAL DELIVERY
(7) INTERLOCK DATA TRANSFER INDICATION

Fig. 7

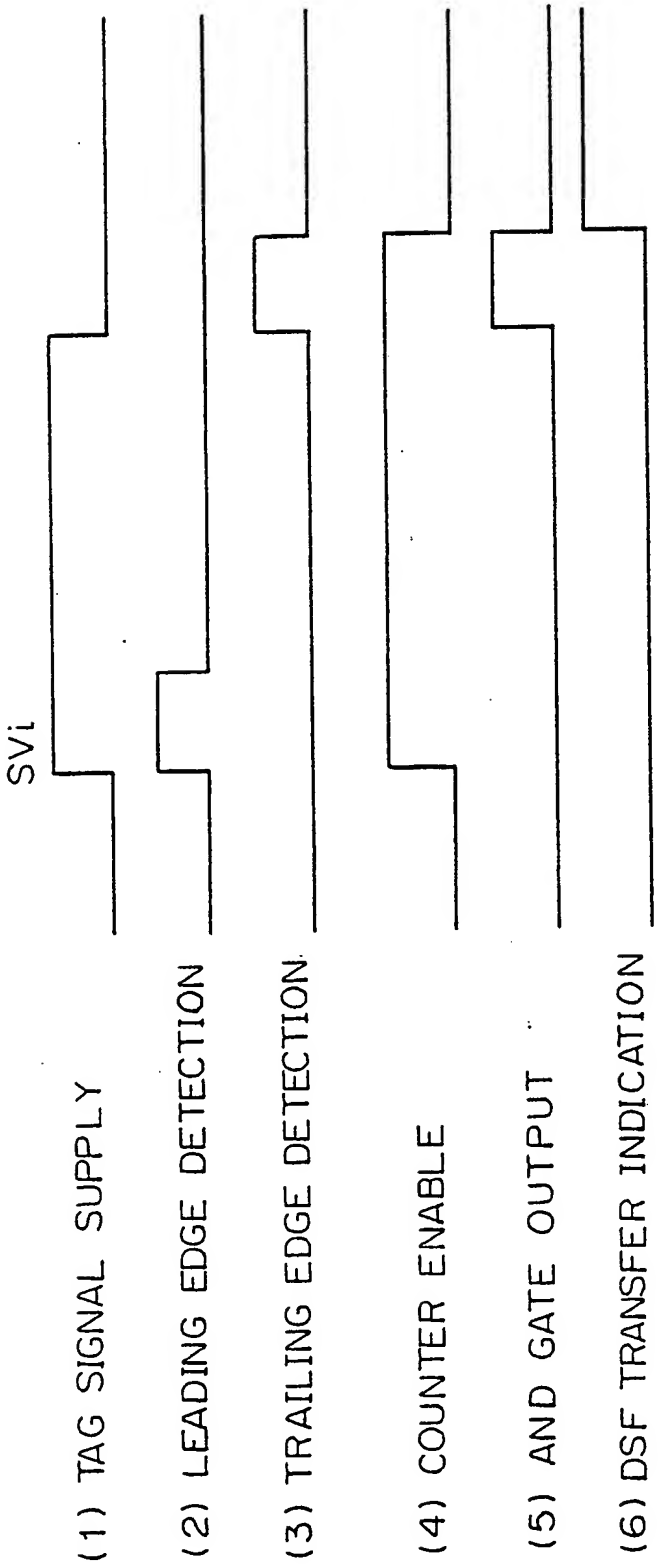

SVi
(1) TAG SIGNAL SUPPLY
(2) LEADING EDGE DETECTION
(3) TRAILING EDGE DETECTION
(4) COUNTER ENABLE
(5) AND GATE OUTPUT
(6) DSF TRANSFER INDICATION

Fig. 8

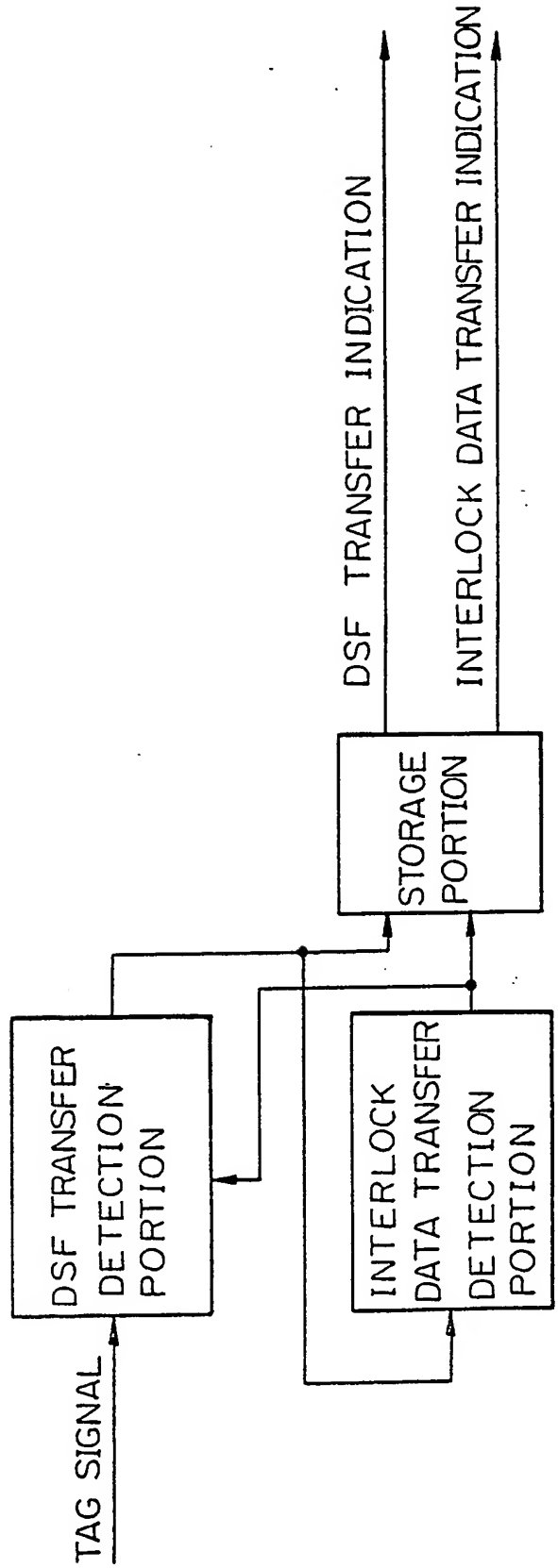
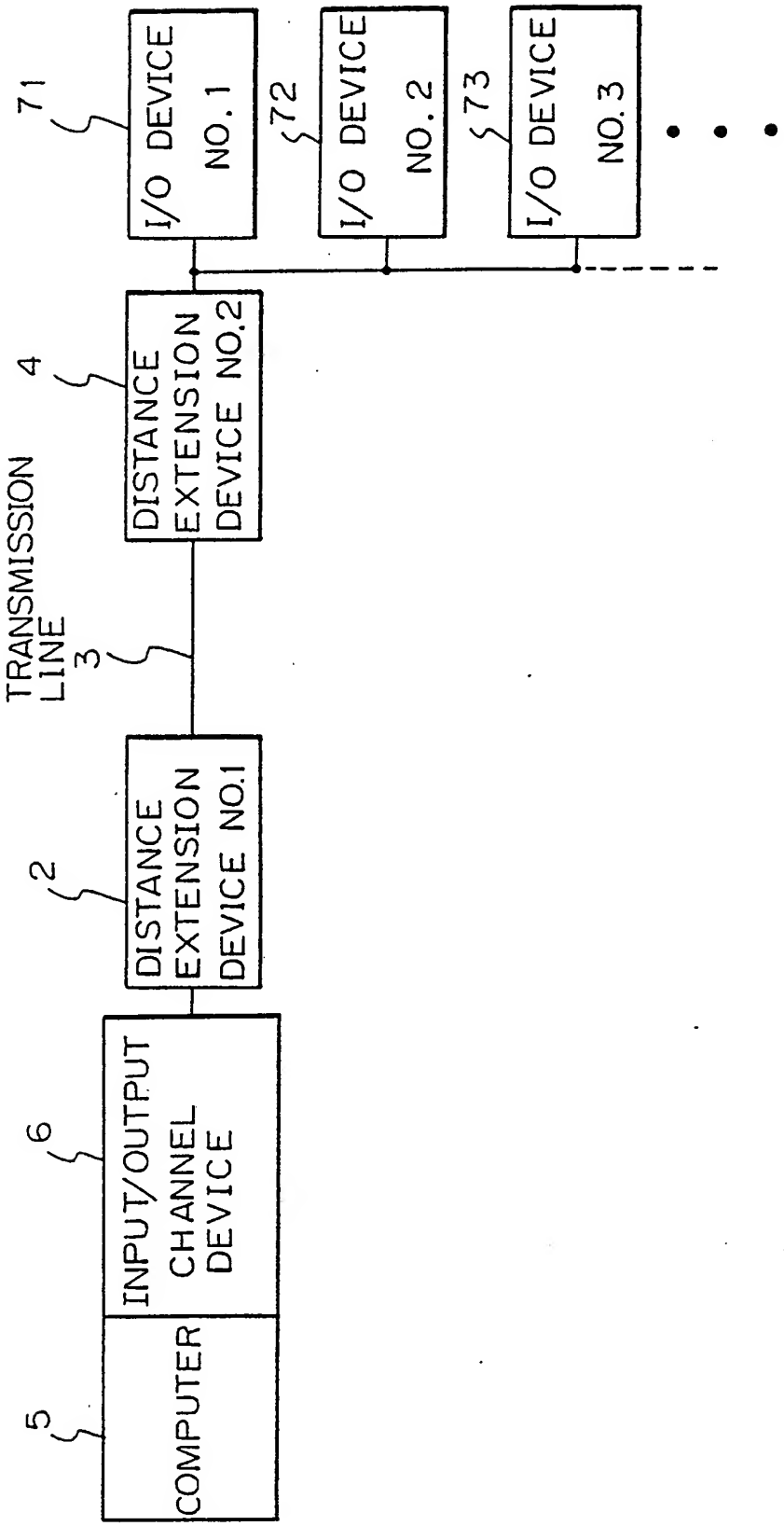

TAG SIGNAL
DSF TRANSFER DETECTION PORTION
INTERLOCK DATA TRANSFER DETECTION PORTION
STORAGE PORTION
DSF TRANSFER INDICATION
INTERLOCK DATA TRANSFER INDICATION

Fig. 9


COMPUTER
5
INPUT/OUTPUT CHANNEL DEVICE
6
DISTANCE EXTENSION DEVICE NO.1
2
TRANSMISSION LINE
3
DISTANCE EXTENSION DEVICE NO.2
4
I/O DEVICE NO.1
71
I/O DEVICE NO.2
72
I/O DEVICE NO.3
73

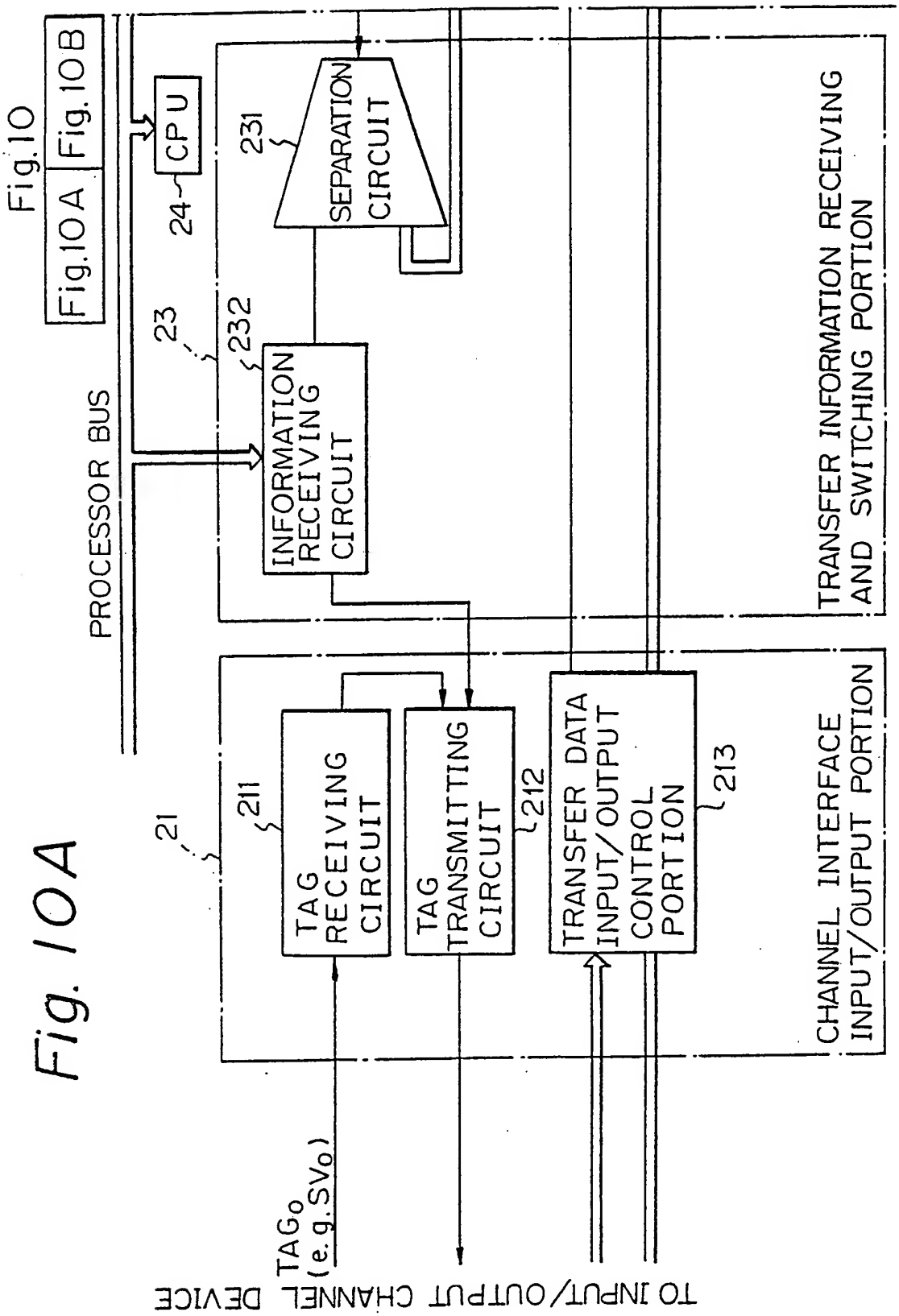


Fig.10
Fig.10A
Fig.10B
CPU
24
231
SEPARATION CIRCUIT
23
232
INFORMATION RECEIVING CIRCUIT
PROCESSOR BUS
TRANSFER INFORMATION RECEIVING AND SWITCHING PORTION
21
211
TAG RECEIVING CIRCUIT
212
TAG TRANSMITTING CIRCUIT
213
TRANSFER DATA INPUT/OUTPUT CONTROL PORTION
CHANNEL INTERFACE INPUT/OUTPUT PORTION
TAGo (e.g.SVo)
TO INPUT/OUTPUT CHANNEL DEVICE

Fig. 10A

Fig. 10B

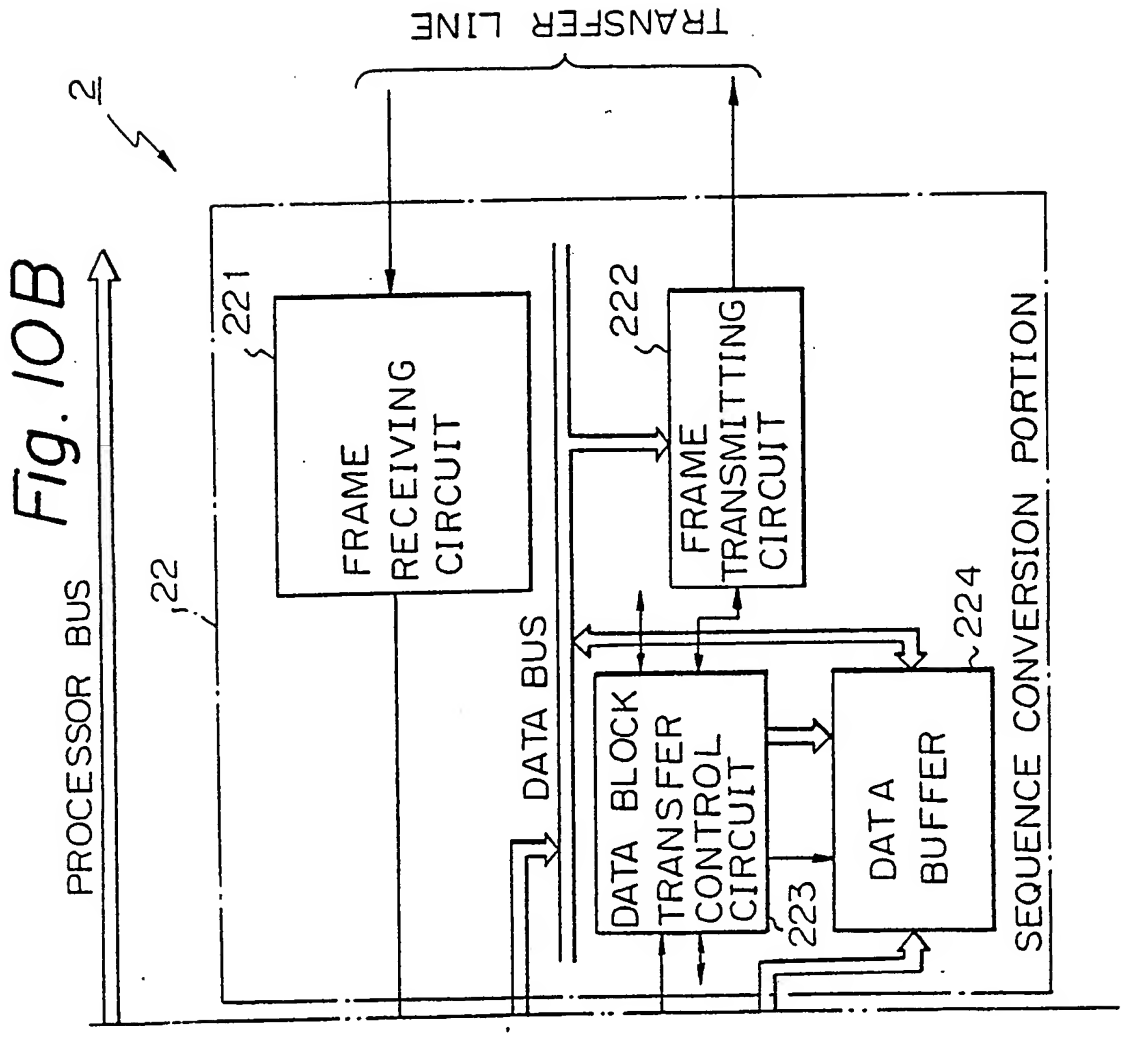

TRANSFER LINE
2
221
FRAME RECEIVING CIRCUIT
222
FRAME TRANSMITTING CIRCUIT
22
PROCESSOR BUS
DATA BUS
DATA BLOCK TRANSFER CONTROL CIRCUIT
223
DATA BUFFER
224
SEQUENCE CONVERSION PORTION

Fig. 11

Fig. 11A	Fig. 11B

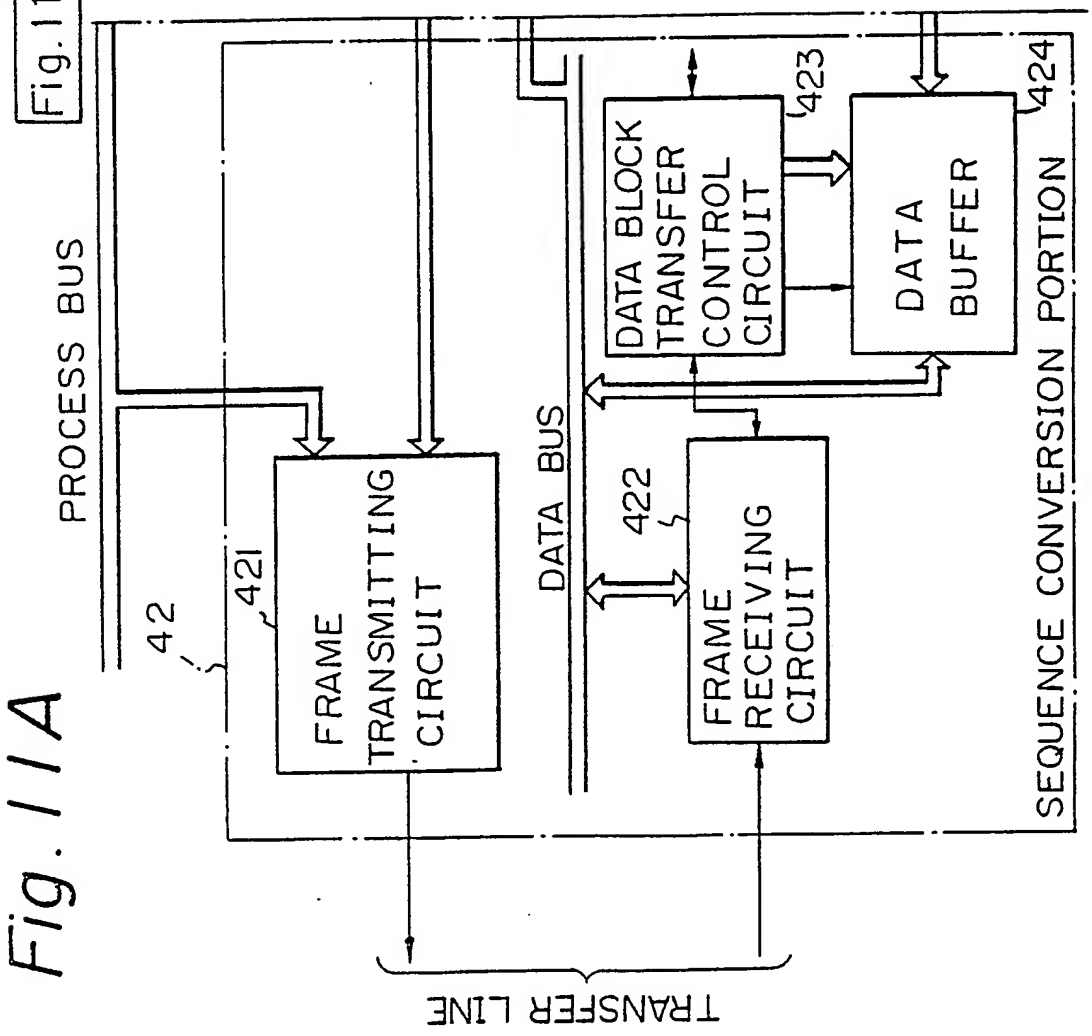


Fig. 11A

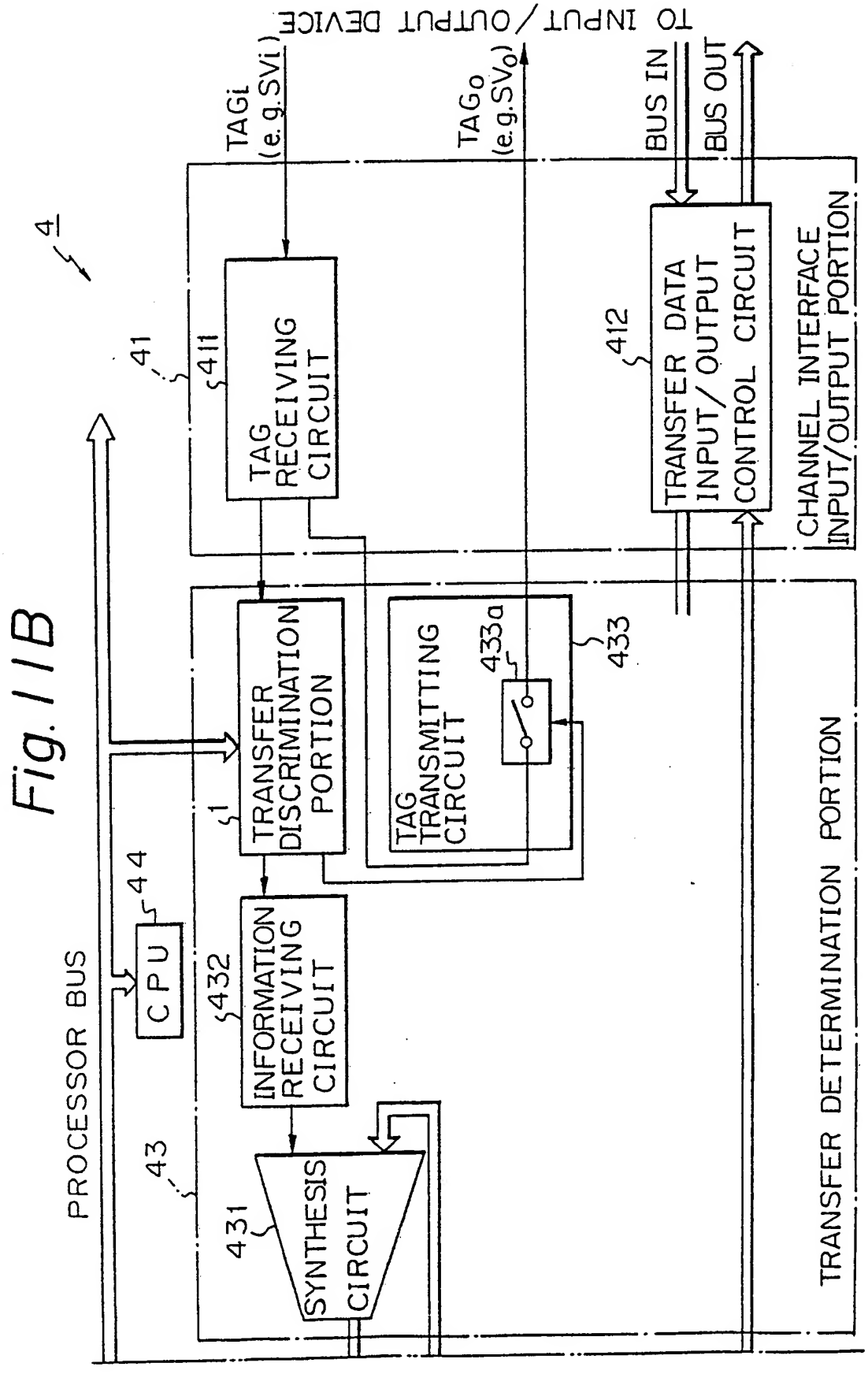

TO INPUT/OUTPUT DEVICE
TAGi (e.g.SVi)
TAGo (e.g.SVo)
BUS IN
BUS OUT
4
41
411
TAG RECEIVING CIRCUIT
412
TRANSFER DATA INPUT/OUTPUT CONTROL CIRCUIT
CHANNEL INTERFACE INPUT/OUTPUT PORTION
TRANSFER DISCRIMINATION PORTION
1
TAG TRANSMITTING CIRCUIT
433a
433
44
CPU
INFORMATION RECEIVING CIRCUIT
432
PROCESSOR BUS
43
431
SYNTHESIS CIRCUIT
TRANSFER DETERMINATION PORTION

Fig. 11B

Fig. 12

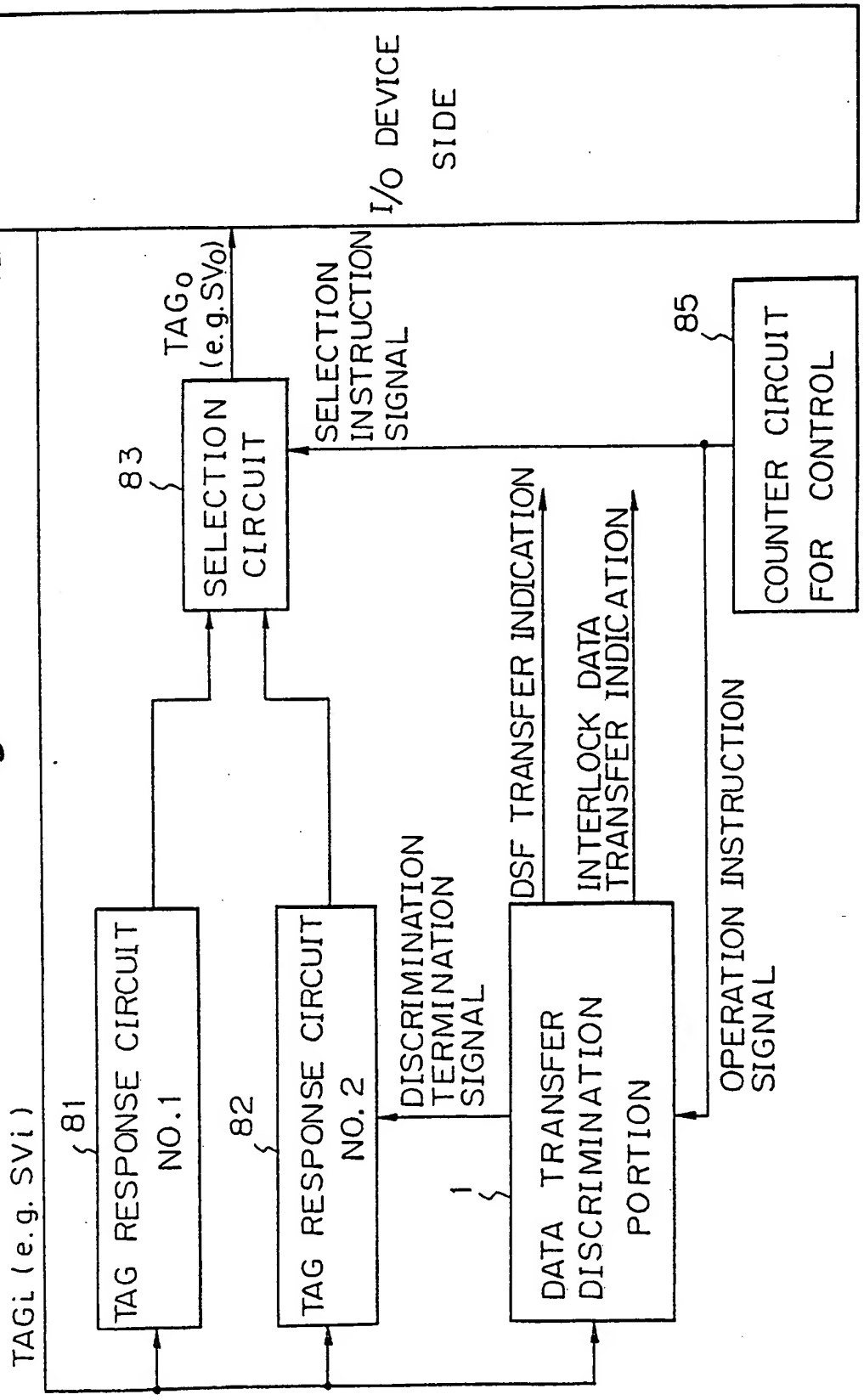

I/O DEVICE SIDE
7
TAGo (e.g. SVo)
SELECTION INSTRUCTION SIGNAL
83
SELECTION CIRCUIT
85
COUNTER CIRCUIT FOR CONTROL
TAGi (e.g. SVi)
81
TAG RESPONSE CIRCUIT NO.1
82
TAG RESPONSE CIRCUIT NO.2
DISCRIMINATION TERMINATION SIGNAL
DSF TRANSFER INDICATION
INTERLOCK DATA TRANSFER INDICATION
1
DATA TRANSFER DISCRIMINATION PORTION
OPERATION INSTRUCTION SIGNAL

Fig. 13 LEADING EDGE DETECTOR

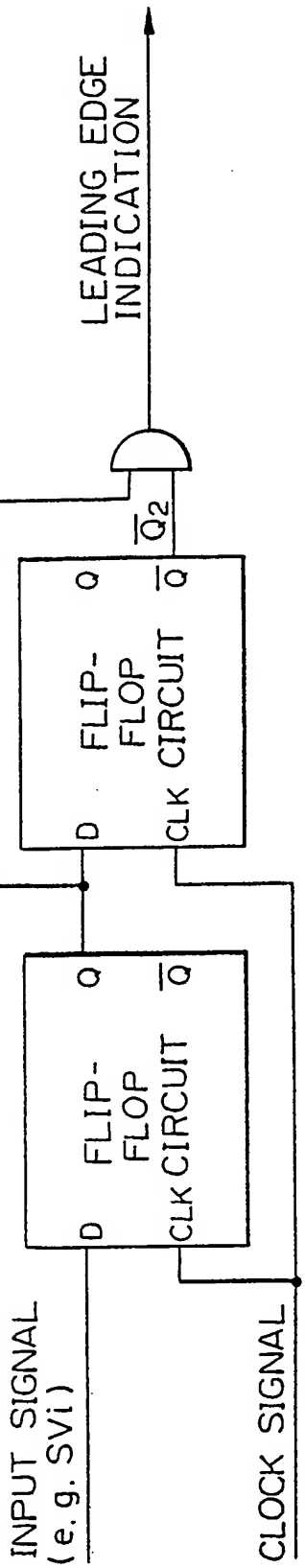


Fig. 14 TRAILING EDGE DETECTOR

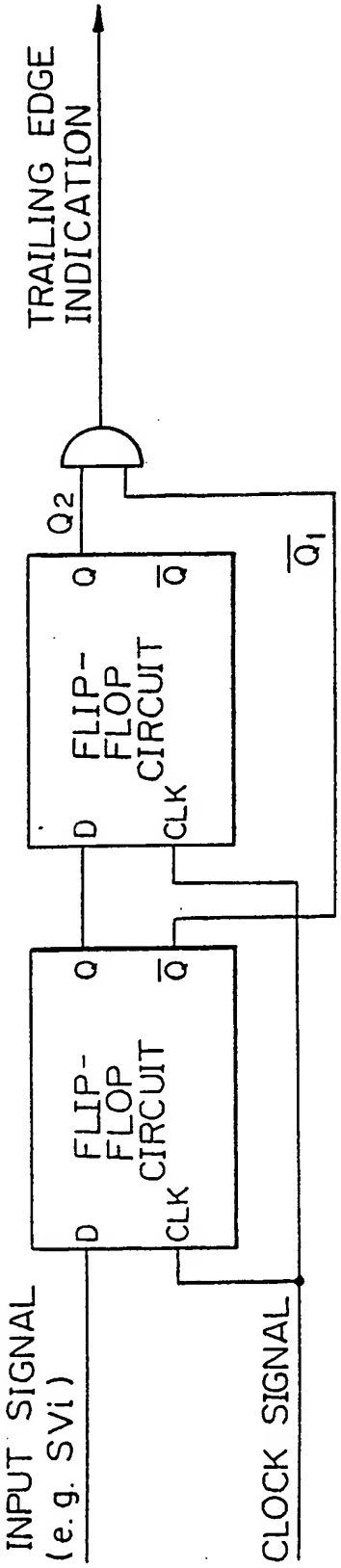


Fig. 15

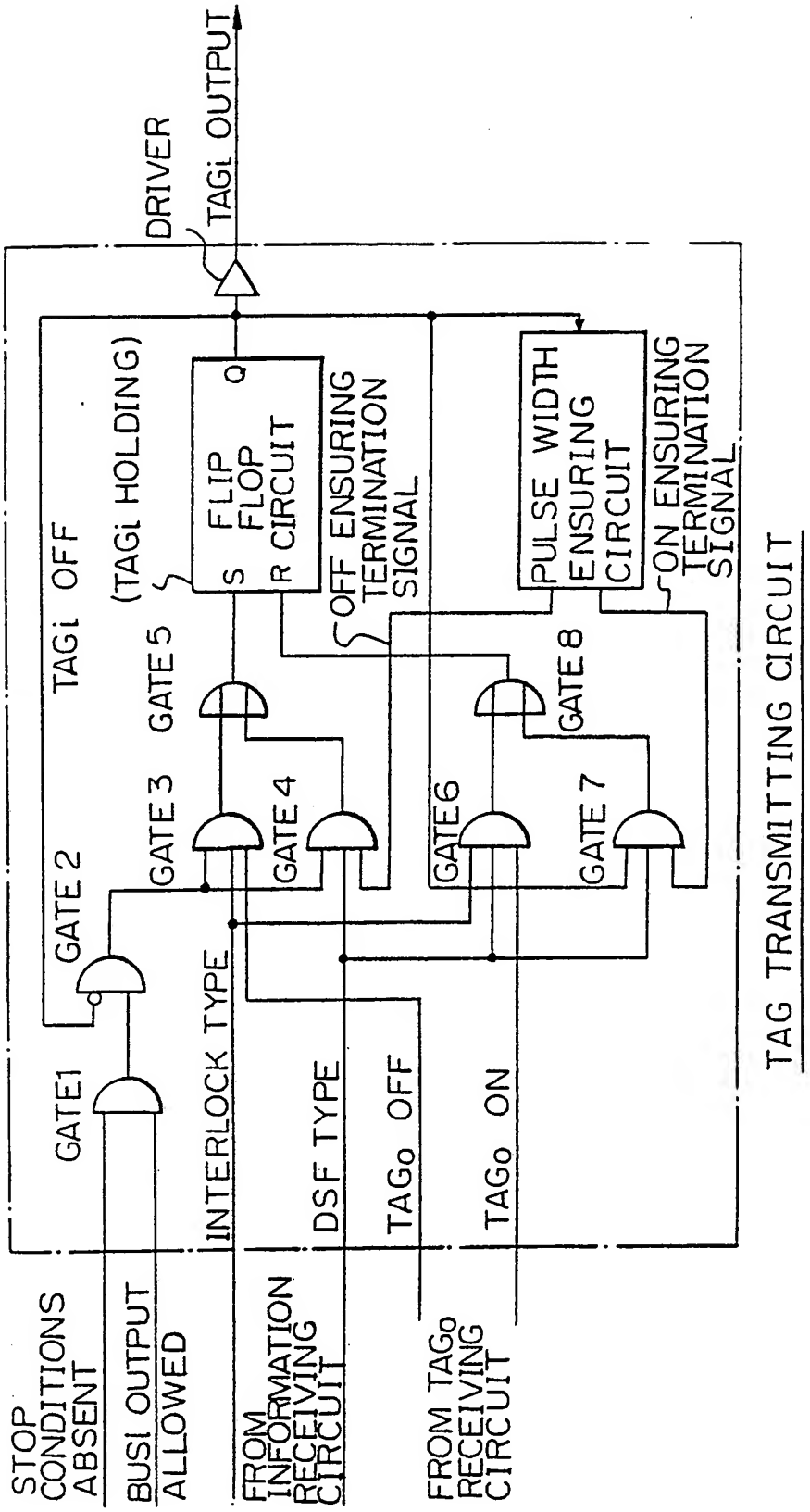

TAG TRANSMITTING CIRCUIT
DRIVER
TAGi OUTPUT
TAGi OFF
(TAGi HOLDING)
S FLIP FLOP R CIRCUIT Q
OFF ENSURING TERMINATION SIGNAL
PULSE WIDTH ENSURING CIRCUIT
ON ENSURING TERMINATION SIGNAL
GATE1
GATE2
GATE3
GATE4
GATE5
GATE6
GATE7
GATE8
INTERLOCK TYPE
DSF TYPE
TAGo OFF
TAGo ON
STOP CONDITIONS ABSENT
BUSI OUTPUT ALLOWED
FROM INFORMATION RECEIVING CIRCUIT
FROM TAGo RECEIVING CIRCUIT

Fig. 16

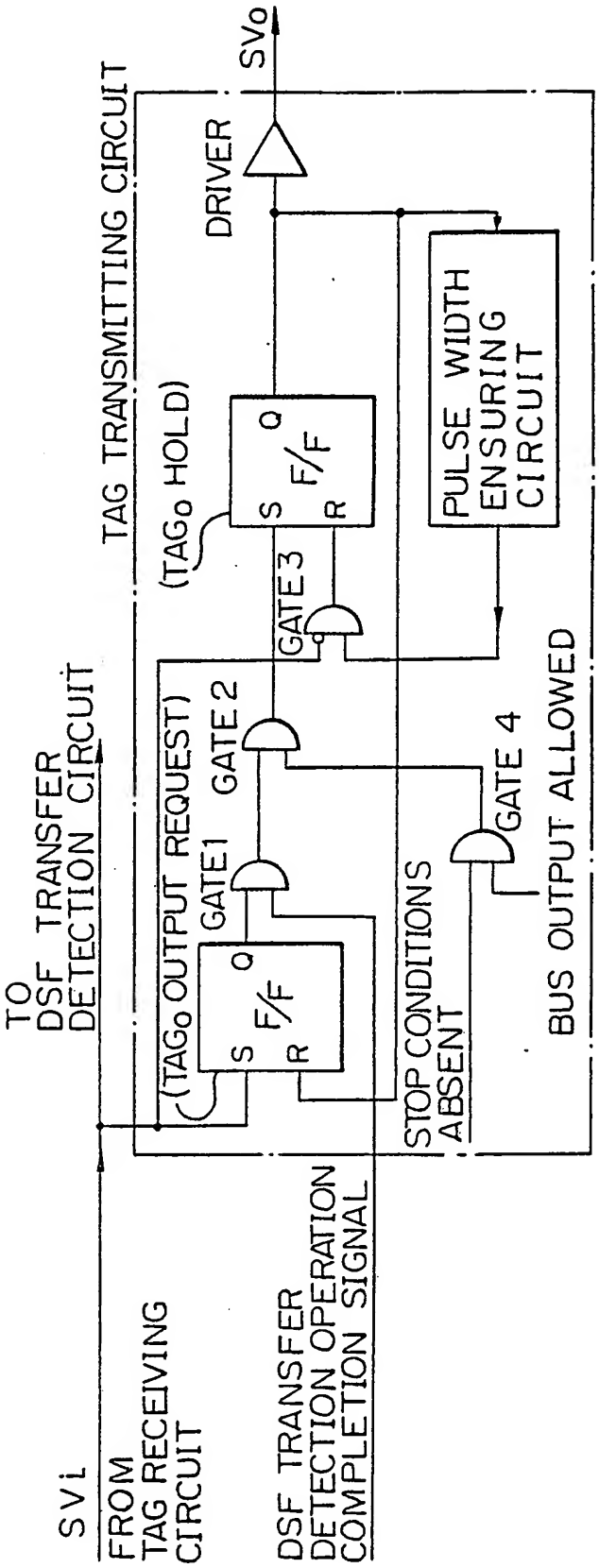

SVi
FROM TAG RECEIVING CIRCUIT
TO DSF TRANSFER DETECTION CIRCUIT
TAG TRANSMITTING CIRCUIT
SVo
DRIVER
(TAG$_O$ OUTPUT REQUEST)
GATE1
GATE 2
(TAG$_O$ HOLD)
GATE 3
GATE 4
F/F
S
R
Q
PULSE WIDTH ENSURING CIRCUIT
STOP CONDITIONS ABSENT
BUS OUTPUT ALLOWED
DSF TRANSFER DETECTION OPERATION COMPLETION SIGNAL

Fig. 17

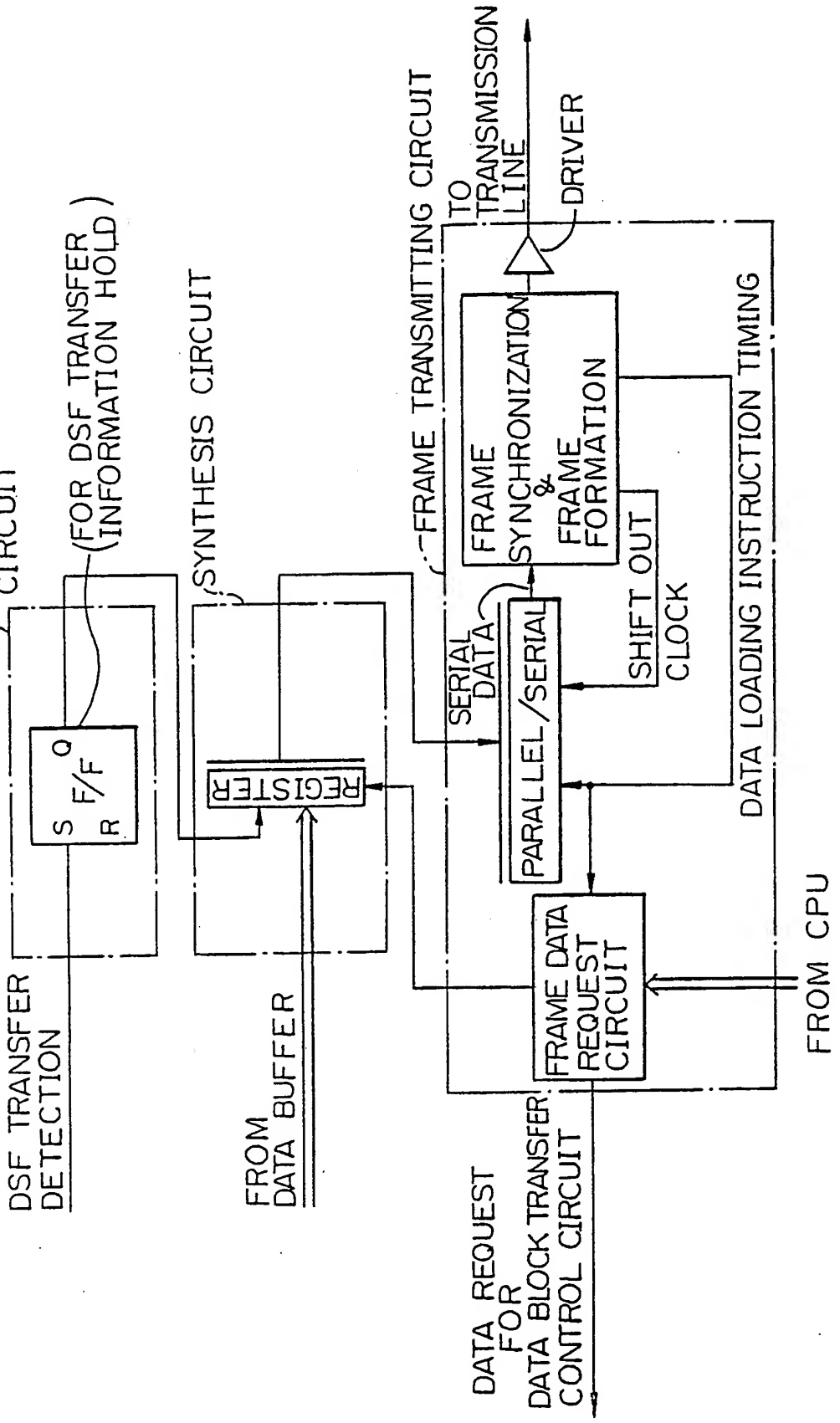
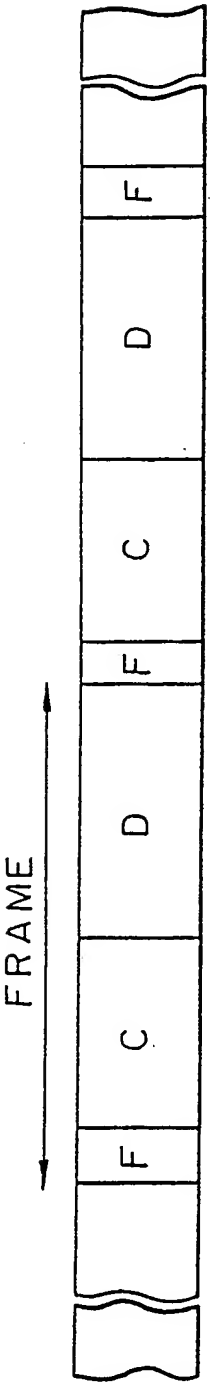

INFORMATION RECEIVING CIRCUIT
(FOR DSF TRANSFER INFORMATION HOLD)
SYNTHESIS CIRCUIT
FRAME TRANSMITTING CIRCUIT
TO TRANSMISSION LINE
DRIVER
FRAME SYNCHRONIZATION & FRAME FORMATION
SERIAL DATA
PARALLEL/SERIAL
SHIFT OUT CLOCK
DATA LOADING INSTRUCTION TIMING
S F/F Q R
REGISTER
DSF TRANSFER DETECTION
FROM DATA BUFFER
FRAME DATA REQUEST CIRCUIT
FROM CPU
DATA REQUEST FOR DATA BLOCK TRANSFER CONTROL CIRCUIT

Fig. 18

SIGNAL FRAME FOR TRANSMISSION



F : FOR FRAME SYNCHRONIZATION
C : CONTROL PORTION, DATA PORTION NATURE INDICATION, COMMUNICATION BETWEEN 1ST & 2ND DEVICES
D : TRANSMISSION OF DATA PORTION, TRANSFER DATA etc.

Fig. 19

Fig. 19A	Fig. 19B

Fig. 19A

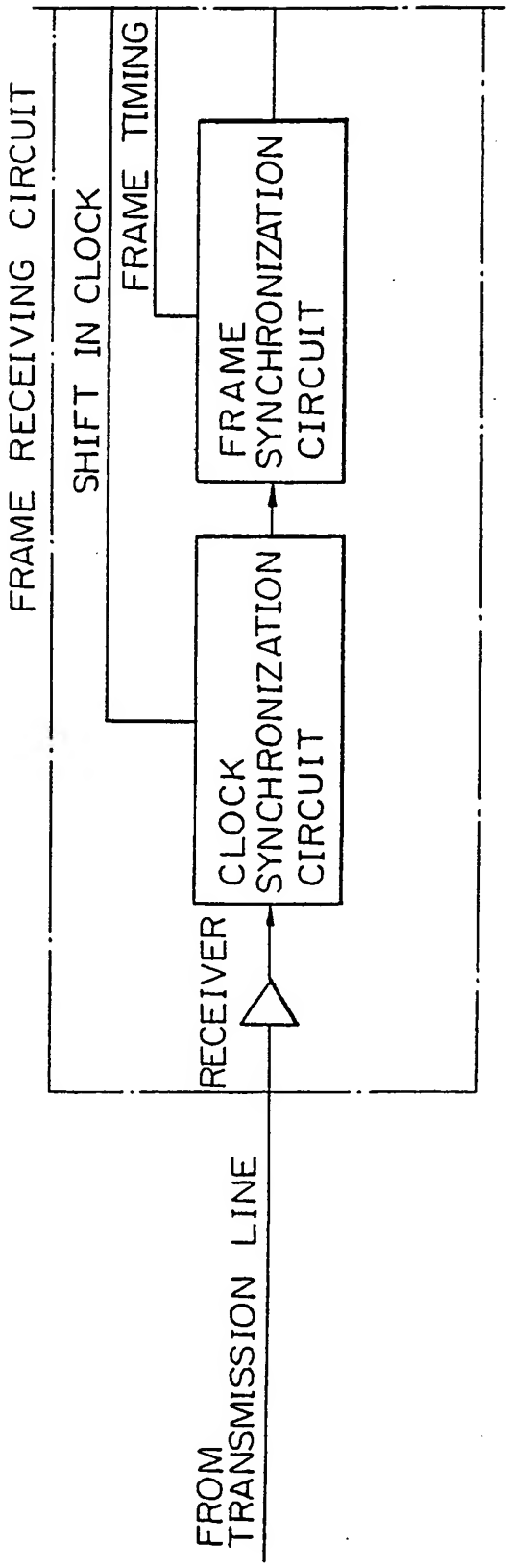
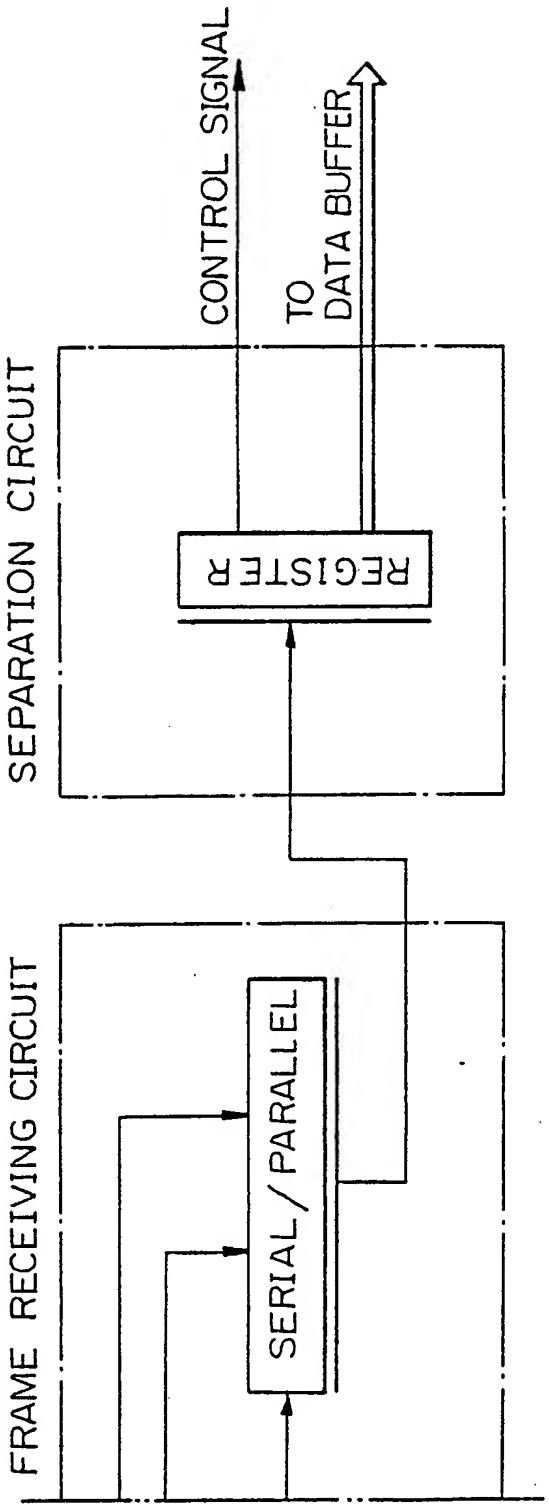


Fig. 19 B


FRAME RECEIVING CIRCUIT
SERIAL / PARALLEL
SEPARATION CIRCUIT
REGISTER
CONTROL SIGNAL
TO DATA BUFFER

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP 87/00787

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 13/42

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	EP, A, 0191334 (IBM) 20 August 1986 see abstract; page 3, lines 66-68; page 4, lines 63-66; page 5, lines 1-5, 18-25; page 6, lines 40-53; page 7, lines 53-62; figures 1-5	1,2,6,9-11
Y	--	12-14
Y	IBM Techical Disclosure Bulletin, volume 24, no. 5, October 1981, (New York, US), S.R. Firth et al.: "Dynamic data streaming/DC interlock control for a multipath channel-to-channel adapter", pages 2621-2622 see page 2621, lines 1-7; page 2622, lines 28-36	1,2,6,9
	--	
Y	Patent Abstracts of Japan, volume 9, no. 257 (P-396)(1980), 15 October 1985, & JP, A, 60107163 (FUJITSU K.K.) 12 June 1985 see the abstract and figure	1,2,6,9
	--	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
8th December 1987	15 FEB 1988
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	E.E. VAN DER PUTTEN

International Application No. PCT/JP 87/00787

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relavant to Claim No
Y	US, A, 4534011 (ANDREWS et al.) 6 August 1985 see page 4, lines 56-62; figure 13 --	12-14
A	EP, A, 0111123 (SIEMENS) 20 June 1984 see page 10, lines 11-14; page 13, lines 16-30 --	1,9
A	IBM Techical Disclosure Bulletin, volume 19, no. 8, January 1977, (New York, US), K.R. Lynch et al.: "Serial channel to I/O interface", pages 3139-3143 see page 3141, lines 1-23	11

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. JP 8700787 SA 19049

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 11/02/88
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0191334	20-08-86	JP-A- 61187057	20-08-86
		US-A- 4712176	08-12-87
US-A- 4534011	06-08-85	JP-A- 58134325	10-08-83
		AU-A- 1078483	11-08-83
		CA-A- 1184313	19-03-85
		AU-B- 552910	26-06-86
EP-A- 0111123	20-06-84	DE-C- 3239997	12-04-84